

REV: 1.01

TITLE

SHEET

TITLE

<i>Gigabyte Technology</i>			
Title			
Cover Sheet			
Size Custom	Document Number	GA-H55M-UD2H	Rev 1.01
Date:	Wednesday, November 04, 2009	Sheet 1 of 35	

GA-H55M-UD2H Version: 1.01

Component value change history

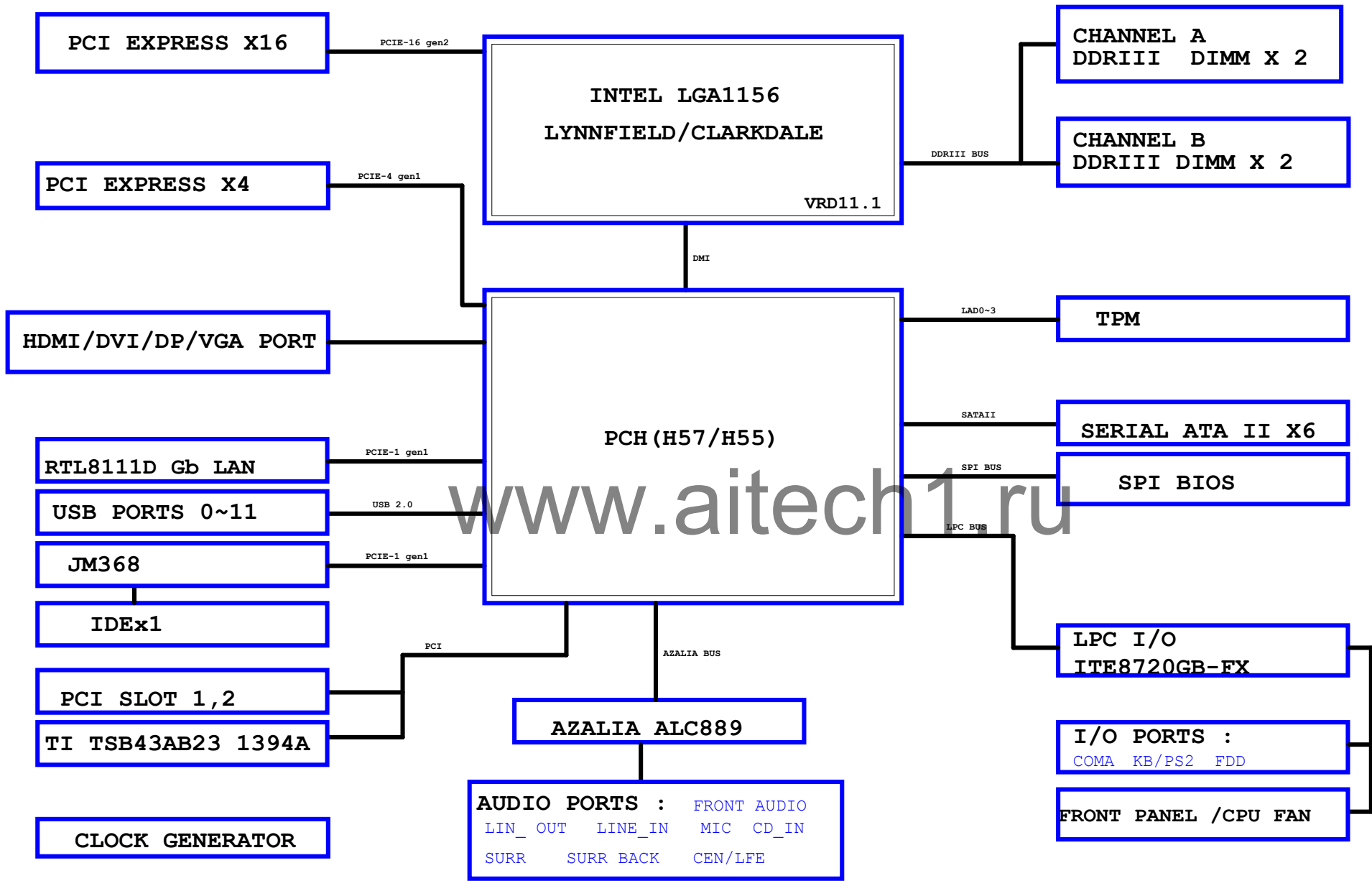
2009/12/08

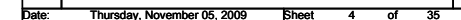
[illegible]

Circuit or PCB layout change
for next version

[illegible]

BLOCK DIAGRAM





40 -SYS_RST <-SYS_RST [13.22.27.28]
 40 R192 49.9/4/1X PECL
 40 R201 49.9/4/1 -THRMTRIP
 33 R178 49.9/4/1 PROCHOT
 34 R182 49.9/4/1X CPUFWROK
 39

LGA1156A			
MAAA0	AW18	SA_MA[0]	AK3 DQSA0
MAAA1	AY15	SA_MA[1]	AK3 -DQSA0
MAAA2	AV15	SA_MA[2]	AK2 DMA0
MAAA3	AU15	SA_MA[3]	
MAAA4	AW14	SA_MA[4]	AH1 MDA0
MAAA5	AY13	SA_MA[5]	AJ4 MDA1
MAAA6	AV14	SA_MA[6]	AL2 MDA2
MAAA7	AW13	SA_MA[7]	AL1 MDA3
MAAA8	AU14	SA_MA[8]	AG2 MDA4
MAAA9	AW12	SA_MA[9]	AH2 MDA5
MAAA10	AT19	SA_MA[10]	AK1 MDA6
MAAA11	AU11	SA_MA[11]	AK2 MDA7
MAAA12	AW11	SA_MA[12]	
MAAA13	AU24	SA_MA[13]	AP2 DQSA1
MAAA14	AT11	SA_MA[14]	AP3 -DQSA1
MAAA15	AR10	SA_MA[15]	AN1 DMA1
[7] -SWEA	AT22	SA_WE#	AN3 MDA8
[7] -SCASA	AU22	SA_DO[8]	AN2 MDA9
[7] -SRASA	AT20	SA_DO[9]	AR3 MDA10
		SA_DO[10]	AR2 MDA11
[7] SBAA0	AV20	SA_BS[0]	AM3 MDA12
[7] SBAA1	AU19	SA_BS[1]	AM2 MDA13
[7] SBAA2	AU12	SA_BS[2]	AP1 MDA14
		SA_DO[15]	AR4 MDA15
[7] -CSA0	AV21	SA_CS#	
[7] -CSA1	AW24	SA_CS#	AL4 DQSA2
[7] -CSA2	AU21	SA_CS#	AL3 -DQSA2
[7] -CSA3	AU23	SA_CS#	AL1 DMA2
[7] CKEA0	AU10	SA_CKE[0]	AT4 MDA16
[7] CKEA1	AW10	SA_CKE[1]	AJ2 MDA17
[7] CKEA2	AV10	SA_CKE[2]	AW3 MDA18
[7] CKEA3	AY10	SA_CKE[3]	AW4 MDA19
		SA_DO[20]	AT3 MDA20
MODT_A0	AV23	SA_ODT[0]	AT1 MDA21
MODT_A1	AV24	SA_ODT[1]	AV2 MDA22
MODT_A2	AW23	SA_ODT[2]	SA_DO[22]
MODT_A3	AY24	SA_ODT[3]	SA_DO[23]
		SA_DO[30]	AY6 DQSA3
[7] DCLKA0	AR22	SA_CK[0]	AW6 -DQSA3
[7] -DCLKA0	AR21	SA_CK#	AW6 DMA3
[7] DCLKA1	AP18	SA_CK#	
[7] -DCLKA1	AN18	SA_CK[1]	SA_DO[24]
[7] DCLKA2	AN21	SA_CK#	AW5 MDA24
[7] -DCLKA2	AP21	SA_CK#	AY5 MDA25
[7] DCLKA3	AP19	SA_CK#	AJ8 MDA26
[7] -DCLKA3	AN19	SA_CK#	AY8 MDA27
		SA_DO[28]	AJ5 MDA28
[7,8] -DDR3_RST	AV8	SM_DRAMRST#	AW6 MDA29
			AV7 MDA30
			AW7 MDA31
TP1	AK22	SA_CS#	AR28 DQSA4
TP1	AM22	SA_CS#	AT29 -DQSA4
TP1	AL23	SA_CS#	AN29 DMA4
TP1	AK23	SA_CS#	
		SA_DO[32]	AN27 MDA32
		SA_DO[33]	AT28 MDA33
		SA_DO[34]	AP28 MDA34
		SA_DO[35]	AP30 MDA35
		SA_DO[36]	AP27 MDA36
		SA_DO[37]	AR27 MDA37
		SA_DO[38]	AR29 MDA38
		SA_DO[39]	AN30 MDA39
		SA_DO[40]	AV32 DQSA5
		SA_DO[41]	AW32 -DQSA5
		SA_DO[42]	AW31 DMA5
		SA_DO[43]	
		SA_DO[44]	AJ30 MDA40
		SA_DO[45]	AJ31 MDA41
		SA_DO[46]	AV33 MDA42
		SA_DO[47]	AJ34 MDA43
		SA_DO[48]	AW30 MDA44
		SA_DO[49]	AW32 MDA45
		SA_DO[50]	AJ33 MDA46
		SA_DO[51]	AW33 MDA47
		SA_DO[52]	
		SA_DO[53]	AW36 DQSA6
		SA_DO[54]	AW35 -DQSA6
		SA_DO[55]	AW35 DMA6
		SA_DO[56]	AW35 MDA48
		SA_DO[57]	AY35 MDA49
		SA_DO[58]	AV37 MDA50
		SA_DO[59]	AJ37 MDA51
		SA_DO[60]	AY34 MDA52
		SA_DO[61]	AW34 MDA53
		SA_DO[62]	AW36 MDA54
		SA_DO[63]	AW37 MDA55
		SA_DO[64]	
		SA_DO[65]	AR30 DQSA7
		SA_DO[66]	AR38 -DQSA7
		SA_DO[67]	AT38 DMA7
		SA_DO[68]	
		SA_DO[69]	AT39 MDA56
		SA_DO[70]	AT40 MDA57
		SA_DO[71]	AN38 MDA58
		SA_DO[72]	AN39 MDA59
		SA_DO[73]	AJ38 MDA60
		SA_DO[74]	AJ39 MDA61
		SA_DO[75]	AP39 MDA62
		SA_DO[76]	AP40 MDA63

DDR_A

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LGA1156(10SC1-F01156-01R)

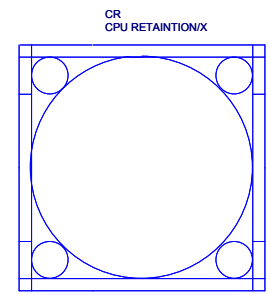
[7] DQSA[0..7]	DQSA[0..7]
[7] -DQSA[0..7]	-DQSA[0..7]
[8] DQSB[0..7]	DQSB[0..7]
[8] -DQSB[0..7]	-DQSB[0..7]
[7] MODT_A[0..3]	MODT_A[0..3]
[8] MODT_B[0..3]	MODT_B[0..3]
[7] MAA[0..15]	MAA[0..15]
[8] MAAB[0..15]	MAAB[0..15]
[7] DMA[0..7]	DMA[0..7]
[8] DMB[0..7]	DMB[0..7]
[7] MDA[0..63]	MDA[0..63]
[8] MDB[0..63]	MDB[0..63]

LGA1156B			
MAAB0	AU20	SB_MA[0]	AF4 DQSB0
MAAB1	AU18	SB_MA[1]	AE5 -DQSB0
MAAB2	AV18	SB_MA[2]	AE4 DMB0
MAAB3	AU17	SB_MA[3]	
MAAB4	AY18	SB_MA[4]	AD7 MDB0
MAAB5	AV17	SB_MA[5]	AD6 MDB1
MAAB6	AW17	SB_MA[6]	AH8 MDB2
MAAB7	AU16	SB_MA[7]	AJ8 MDB3
MAAB8	AT17	SB_MA[8]	AC7 MDB4
MAAB9	AY16	SB_MA[9]	AC6 MDB5
MAAB10	AV15	SB_MA[10]	AF5 MDB6
MAAB11	AW16	SB_MA[11]	AE6 MDB7
MAAB12	AY15	SB_MA[12]	
MAAB13	AW18	SB_MA[13]	AH6 DQSB1
MAAB14	AY12	SB_MA[14]	AJ5 -DQSB1
MAAB15	AV11	SB_MA[15]	AH4 DMB1
		SB_DO[8]	AG5 MDB8
[8] -SWEB	AW26	SB_WE#	AH7 MDB9
[8] -SCASB	AW26	SB_CAS#	AK6 MDB10
[8] -SRASB	AW26	SB_RAS#	AL4 MDB11
[8] SBAB0	AW25	SB_BS[0]	AG6 MDB12
[8] SBAB1	AW25	SB_BS[1]	AC4 MDB13
[8] SBAB2	AW25	SB_BS[2]	AJ7 MDB14
		SB_DO[15]	AK7 MDB15
[8] -CSB0	AY27	SB_CS#	
[8] -CSB1	AW26	SB_CS#	AN6 DQSB2
[8] -CSB2	AW26	SB_CS#	AM6 -DQSB2
[8] -CSB3	AW26	SB_CS#	AM7 DMB2
[8] CKEB0	AW8	SB_CKE[0]	AL6 MDB16
[8] CKEB1	AY9	SB_CKE[1]	AN6 MDB17
[8] CKEB2	AU9	SB_CKE[2]	AP6 MDB18
[8] CKEB3	AV9	SB_CKE[3]	AR5 MDB19
		SB_DO[20]	AL5 MDB20
MODT_B0	AU27	SB_ODT[0]	AM4 MDB21
MODT_B1	AU27	SB_ODT[1]	AN7 MDB22
MODT_B2	AV27	SB_ODT[2]	AP5 MDB23
MODT_B3	AV27	SB_ODT[3]	
		SB_DO[33]	AR8 DQSB3
		SB_DO[34]	AP8 -DQSB3
		SB_DO[35]	AT7 DMB3
[8] DCLKB0	AR17	SB_CK[0]	
[8] -DCLKB0	AR16	SB_CK#	AT6 MDB24
[8] DCLKB1	AT15	SB_CK#	AR7 MDB25
[8] -DCLKB1	AR15	SB_CK[1]	AP9 MDB26
[8] DCLKB2	AN17	SB_CK#	AM8 MDB27
[8] -DCLKB2	AN16	SB_CK#	AN8 MDB28
[8] DCLKB3	AR18	SB_CK#	AR6 MDB29
[8] -DCLKB3	AR18	SB_CK#	AL8 MDB30
		SB_DO[30]	AT9 MDB31
		SB_DO[31]	
TP12	AM23	SB_CS#	AT25 DQSB4
TP13	AM24	SB_CS#	AR24 DQSB4
TP15	AK24	SB_CS#	AT24 DMB4
TP17	AK24	SB_CS#	
		SB_DO[32]	AN23 MDB32
		SB_DO[33]	AP23 MDB33
		SB_DO[34]	AR25 MDB34
		SB_DO[35]	AR26 MDB35
		SB_DO[36]	AT23 MDB36
		SB_DO[37]	AP22 MDB37
		SB_DO[38]	AP25 MDB38
		SB_DO[39]	AT26 MDB39
		SB_DO[40]	
		SB_DO[41]	AP32 DQSB5
		SB_DO[42]	AR32 -DQSB5
		SB_DO[43]	AN32 DMB5
		SB_DO[44]	
		SB_DO[45]	AT32 MDB40
		SB_DO[46]	AP31 MDB41
		SB_DO[47]	AR33 MDB42
		SB_DO[48]	AM32 MDB43
		SB_DO[49]	AT31 MDB44
		SB_DO[50]	AR31 MDB45
		SB_DO[51]	AR34 MDB46
		SB_DO[52]	AT33 MDB47
		SB_DO[53]	
		SB_DO[54]	AR36 DQSB6
		SB_DO[55]	AR37 -DQSB6
		SB_DO[56]	AM33 DMB6
		SB_DO[57]	
		SB_DO[58]	AR35 MDB48
		SB_DO[59]	AT36 MDB49
		SB_DO[60]	AP36 MDB50
		SB_DO[61]	AP36 MDB51
		SB_DO[62]	AP34 MDB52
		SB_DO[63]	AT35 MDB53
		SB_DO[64]	AN34 MDB54
		SB_DO[65]	AP37 MDB55
		SB_DO[66]	
		SB_DO[67]	AL37 DQSB7
		SB_DO[68]	AM36 -DQSB7
		SB_DO[69]	AK35 DMB7
		SB_DO[70]	
		SB_DO[71]	AL35 MDB56
		SB_DO[72]	AM35 MDB57
		SB_DO[73]	AJ36 MDB58
		SB_DO[74]	AJ37 MDB59
		SB_DO[75]	AN35 MDB60
		SB_DO[76]	AM34 MDB61
		SB_DO[77]	AJ35 MDB62
		SB_DO[78]	AL36 MDB63

DDR_B

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LGA1156(10SC1-F01156-01R)



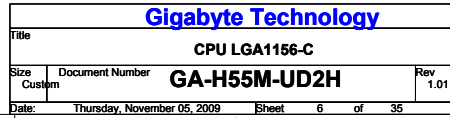
Need check the new CPU ME

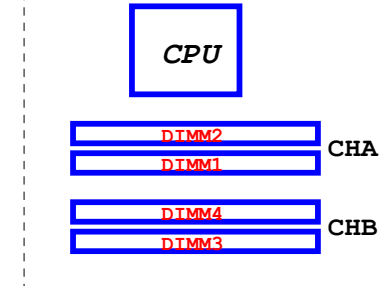
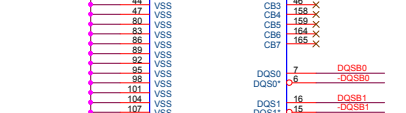
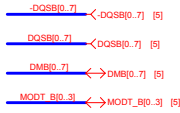
LGA1156_P



PLATE+HLM(12KRC-0F0001-01R)

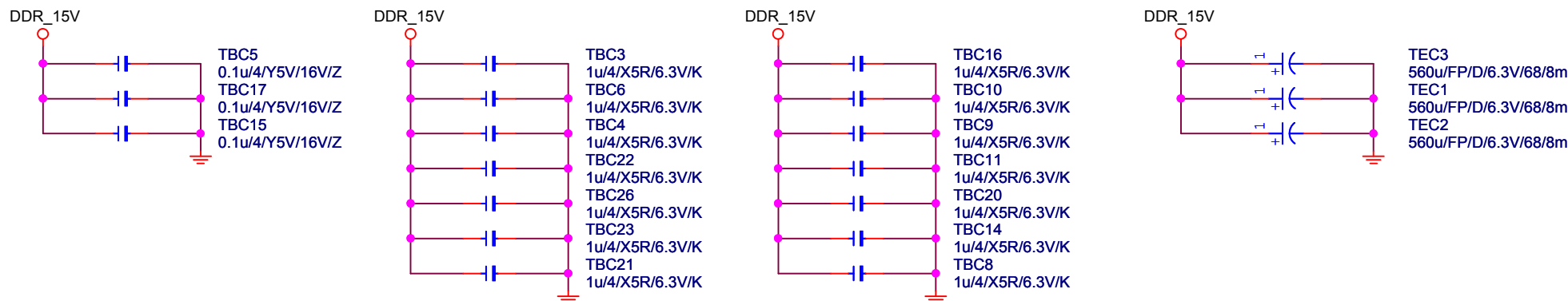
Gigabyte Technology			
Title			
CPU LGA1156-B			
Size			
Custom			
Document Number			
GA-H55M-UD2H			
Date:			
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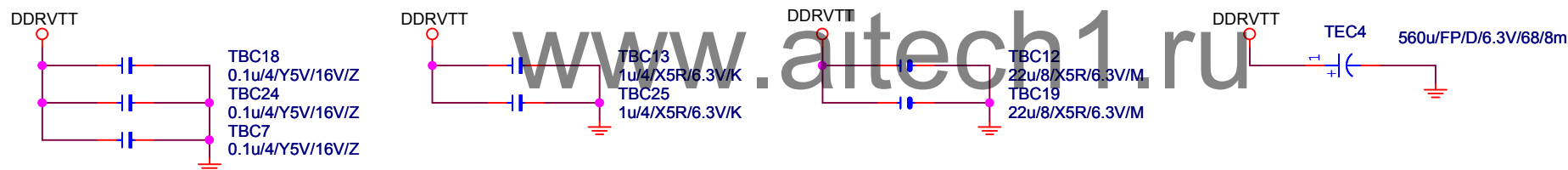


DDR TERMINATION CHANNEL A/B

DDR15V Decouple



DDRVTT Decouple



REF VCC層GND, GND層GND要塞孔

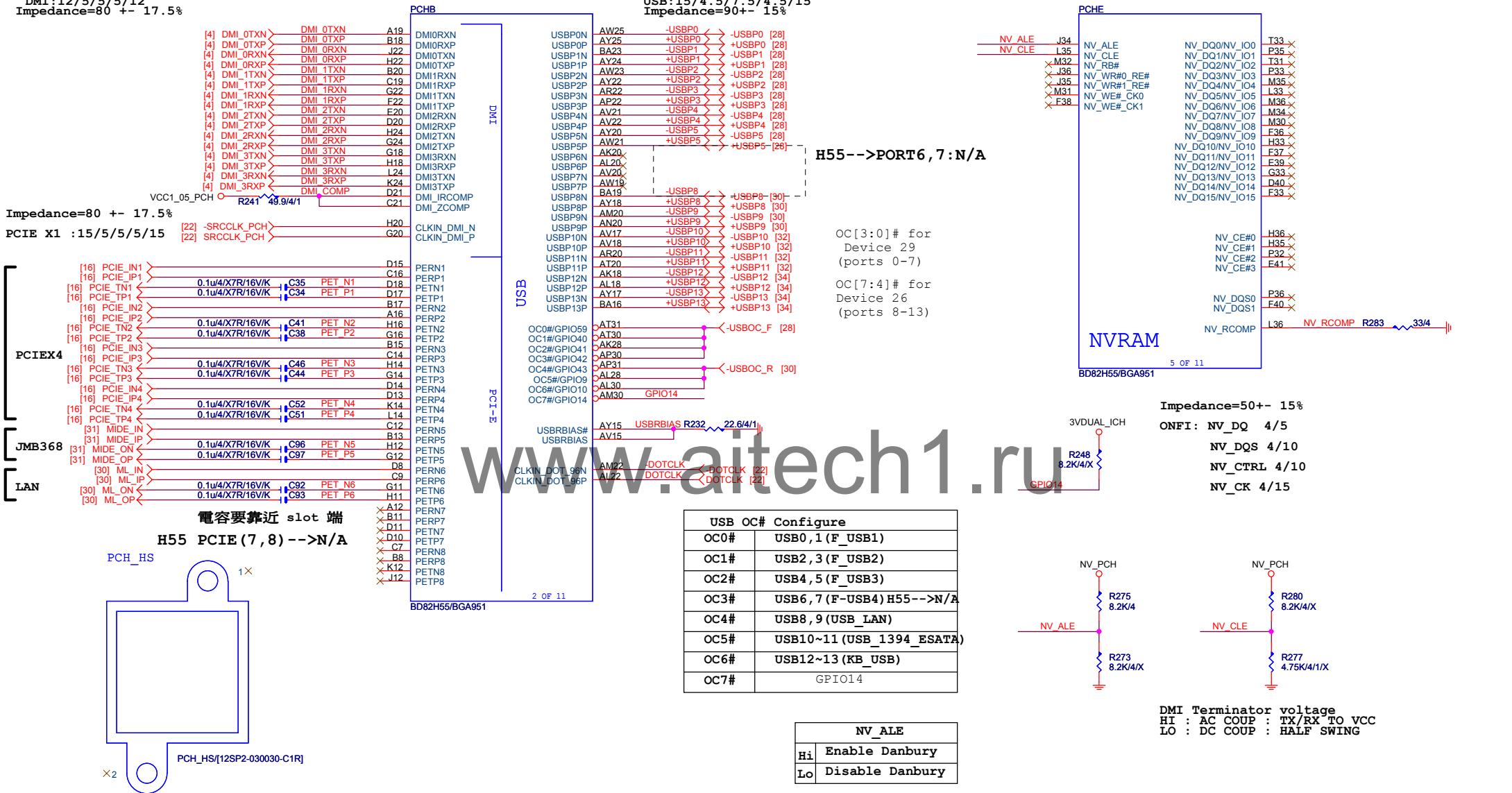


REF GND層GND, VCC層GND要塞孔

Gigabyte Technology		
Title		
DDRIII POWER CAP		
Size A	Document Number	Rev
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DMI:12/5/5/5/12
Impedance=80 +- 17.5%

USB:15/4.5/7.5/4.5/15
Impedance=90+- 15%



Impedance=80 +- 17.5%
PCIE X1 :15/5/5/5/15

PCIE X4

JMB368

LAN

电容要靠近 slot 端
H55 PCIE (7,8) -->N/A

PCH_HS

PCH_HS[12SP2-030030-C1R]

USB OC# Configure	
OC0#	USB0,1 (F_USB1)
OC1#	USB2,3 (F_USB2)
OC2#	USB4,5 (F_USB3)
OC3#	USB6,7 (F_USB4) H55-->N/A
OC4#	USB8,9 (USB_LAN)
OC5#	USB10~11 (USB_1394_ESATA)
OC6#	USB12~13 (KB_USB)
OC7#	GPIO14

NV ALE	
Hi	Enable Danbury
Lo	Disable Danbury

Intel anti theft technolgy

H55-->PORT6,7:N/A

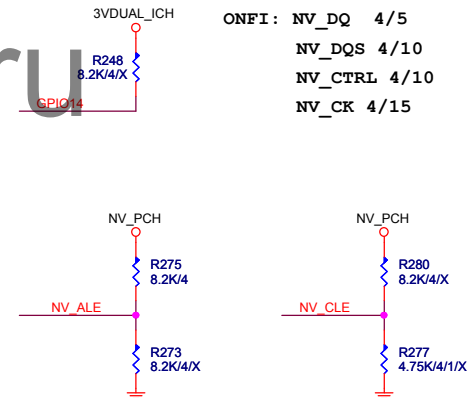
OC[3:0]# for
Device 29
(ports 0-7)

OC[7:4]# for
Device 26
(ports 8-13)

NVRAM

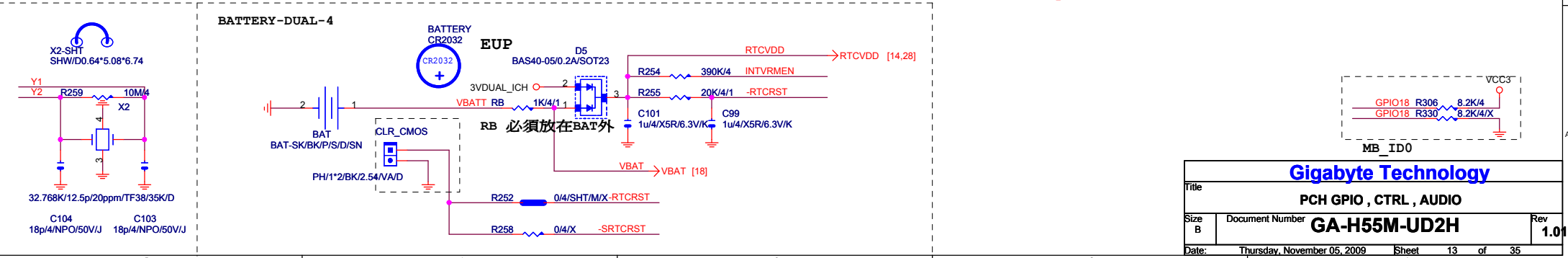
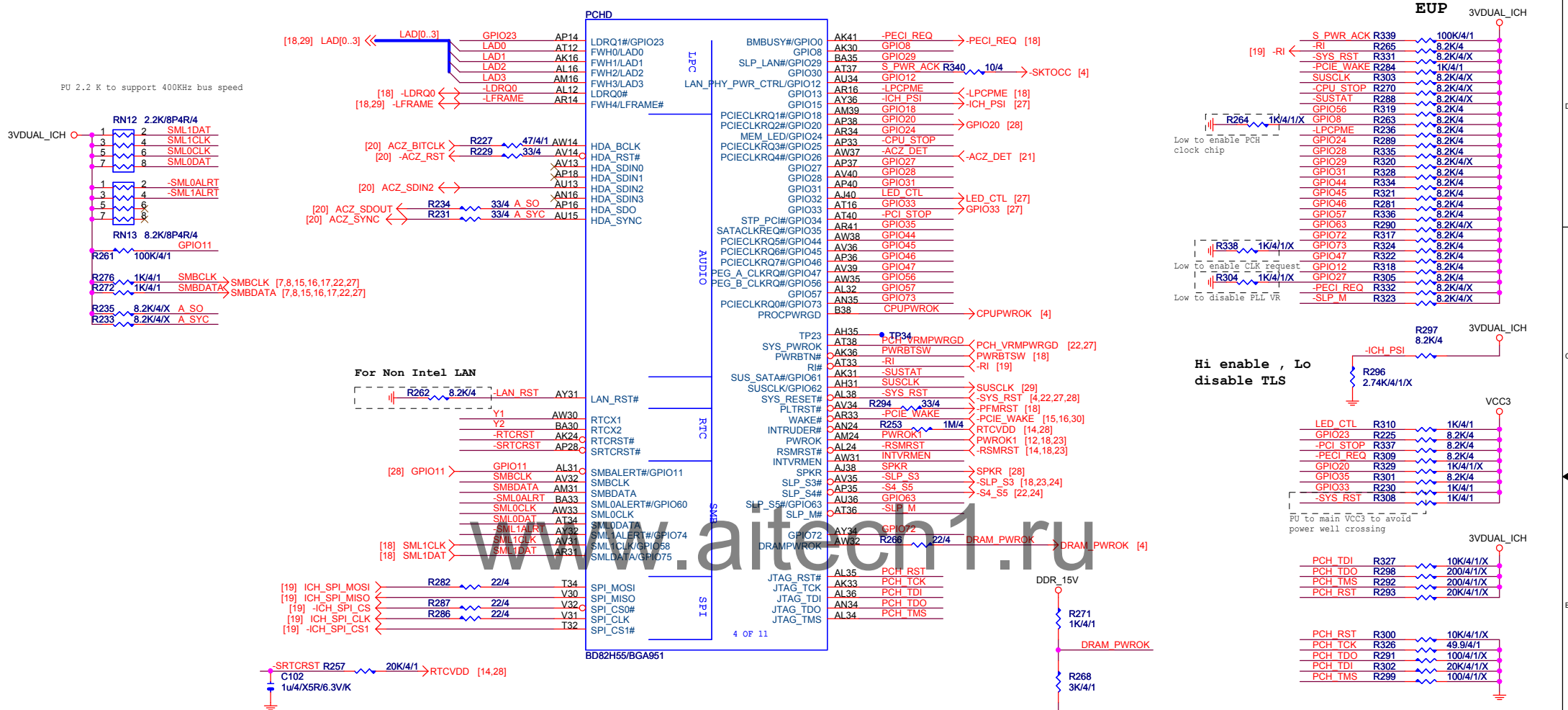
BD82H55/BGA951

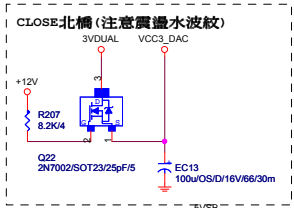
Impedance=50+- 15%
ONFI: NV_DQ 4/5
NV_DQS 4/10
NV_CTRL 4/10
NV_CK 4/15

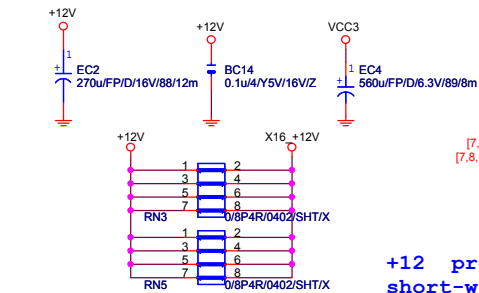


DMI Terminator voltage
HI : AC COUP : TX/RX TO VCC
LO : DC COUP : HALF SWING

Gigabyte Technology		
Title PCH FDI,DMI,USB ,PCIE,NVRAM		
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EXP_RXP[0..15] >> EXP_RXP[0..15] [4]
 EXP_RXN[0..15] >> EXP_RXN[0..15] [4]
 EXP_TXP[0..15] >> EXP_TXP[0..15] [4]
 EXP_TXN[0..15] >> EXP_TXN[0..15] [4]

PCIE16:15/4/8/4/15

EXP_TXP0	C42	0.1u4/X7R/16V/K	EXP_TXP0C
EXP_TXN0	C43	0.1u4/X7R/16V/K	EXP_TXN0C
EXP_TXP1	C45	0.1u4/X7R/16V/K	EXP_TXP1C
EXP_TXN1	C48	0.1u4/X7R/16V/K	EXP_TXN1C
EXP_TXP2	C53	0.1u4/X7R/16V/K	EXP_TXP2C
EXP_TXN2	C54	0.1u4/X7R/16V/K	EXP_TXN2C
EXP_TXP3	C56	0.1u4/X7R/16V/K	EXP_TXP3C
EXP_TXN3	C58	0.1u4/X7R/16V/K	EXP_TXN3C
EXP_TXP4	C59	0.1u4/X7R/16V/K	EXP_TXP4C
EXP_TXN4	C60	0.1u4/X7R/16V/K	EXP_TXN4C
EXP_TXP5	C82	0.1u4/X7R/16V/K	EXP_TXP5C
EXP_TXN5	C83	0.1u4/X7R/16V/K	EXP_TXN5C
EXP_TXP6	C65	0.1u4/X7R/16V/K	EXP_TXP6C
EXP_TXN6	C66	0.1u4/X7R/16V/K	EXP_TXN6C
EXP_TXP7	C67	0.1u4/X7R/16V/K	EXP_TXP7C
EXP_TXN7	C68	0.1u4/X7R/16V/K	EXP_TXN7C
EXP_TXP8	C69	0.1u4/X7R/16V/K	EXP_TXP8C
EXP_TXN8	C70	0.1u4/X7R/16V/K	EXP_TXN8C
EXP_TXP9	C71	0.1u4/X7R/16V/K	EXP_TXP9C
EXP_TXN9	C72	0.1u4/X7R/16V/K	EXP_TXN9C
EXP_TXP10	C74	0.1u4/X7R/16V/K	EXP_TXP10C
EXP_TXN10	C76	0.1u4/X7R/16V/K	EXP_TXN10C
EXP_TXP11	C77	0.1u4/X7R/16V/K	EXP_TXP11C
EXP_TXN11	C78	0.1u4/X7R/16V/K	EXP_TXN11C
EXP_TXP12	C80	0.1u4/X7R/16V/K	EXP_TXP12C
EXP_TXN12	C82	0.1u4/X7R/16V/K	EXP_TXN12C
EXP_TXP13	C84	0.1u4/X7R/16V/K	EXP_TXP13C
EXP_TXN13	C86	0.1u4/X7R/16V/K	EXP_TXN13C
EXP_TXP14	C87	0.1u4/X7R/16V/K	EXP_TXP14C
EXP_TXN14	C89	0.1u4/X7R/16V/K	EXP_TXN14C
EXP_TXP15	C91	0.1u4/X7R/16V/K	EXP_TXP15C
EXP_TXN15	C94	0.1u4/X7R/16V/K	EXP_TXN15C

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

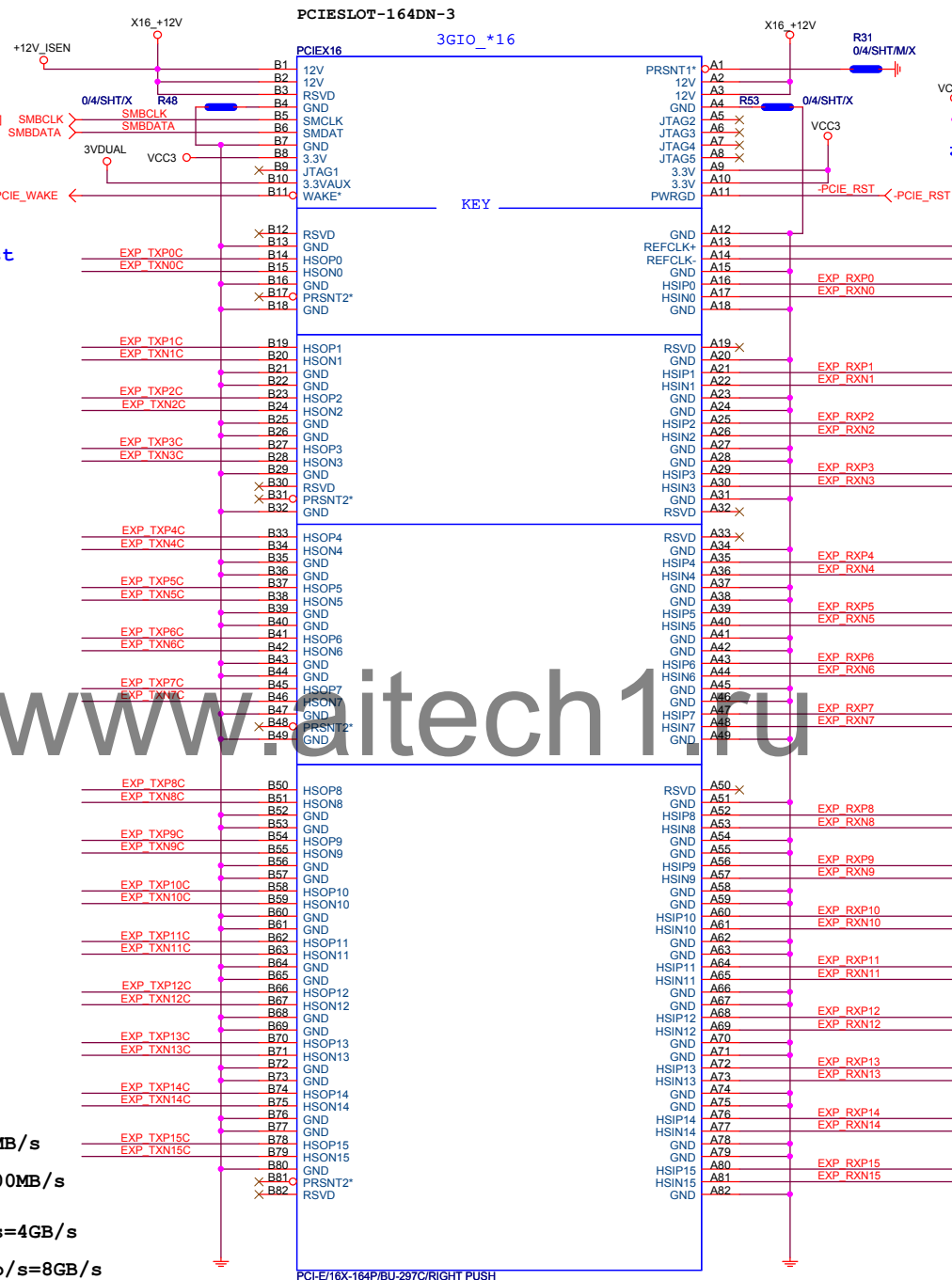
PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b) X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b) X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b) X16X2=64Gb/s=8GB/s

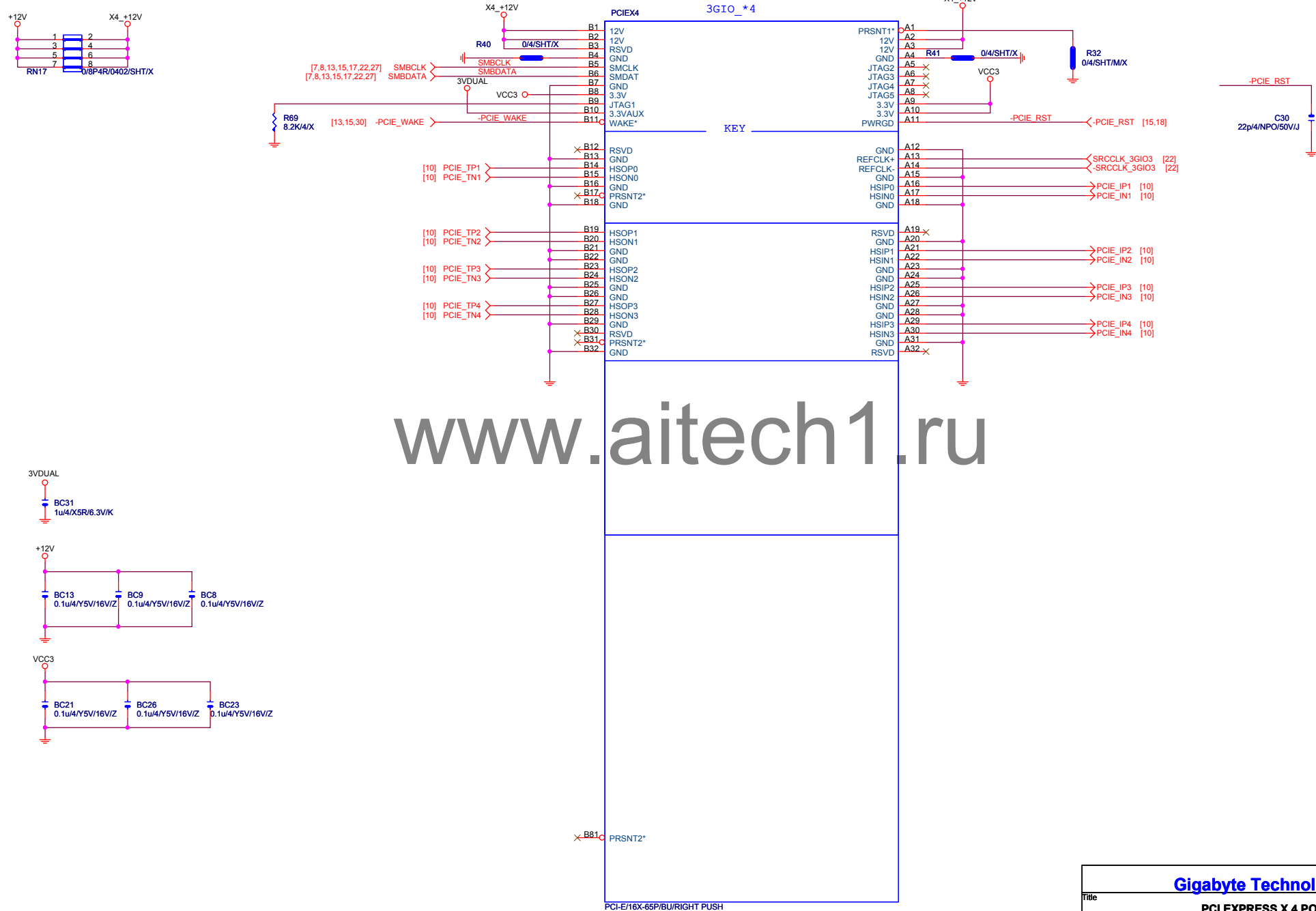
PCI-E REV:2.0--> 5GHZ

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Gigabyte Technology		
Title PCI EXPRESS * 16		
Size Custom	Document Number GA-H55M-UD2H	Rev 1.01
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PCIESLOT-64D-98D-1

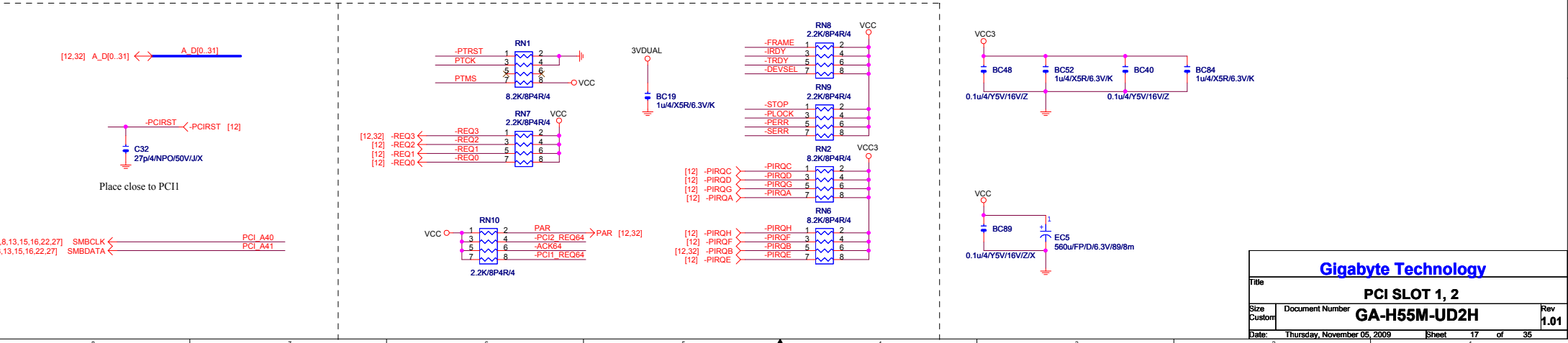
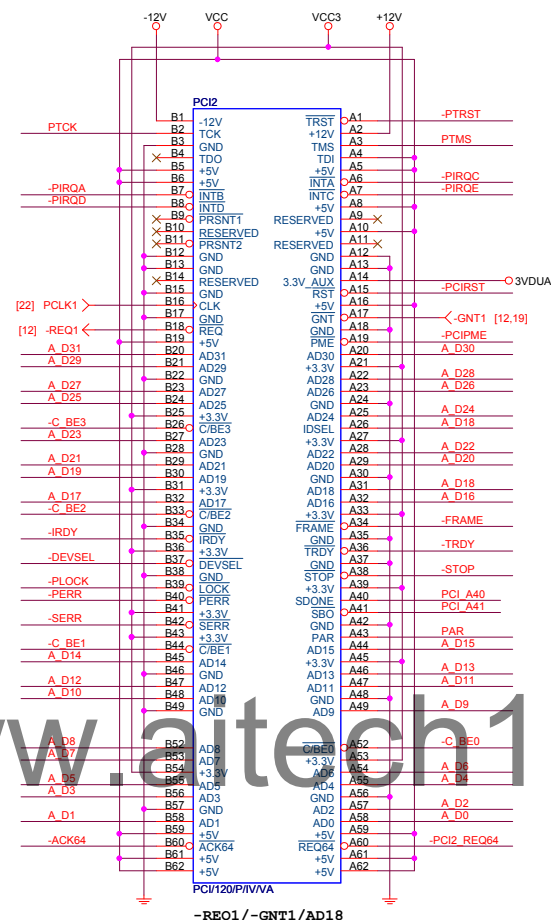
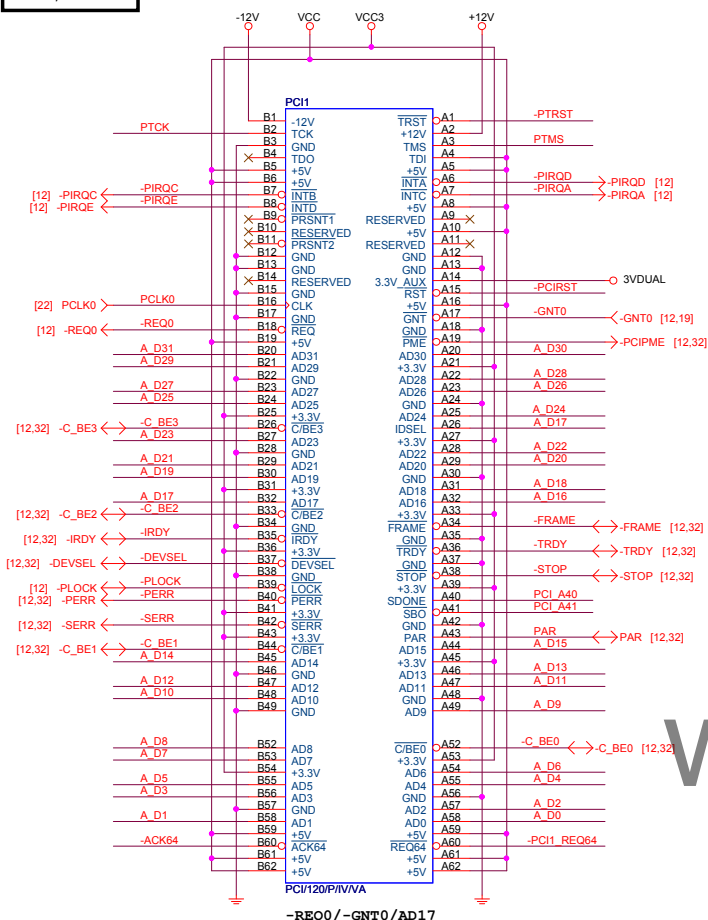


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Gigabyte Technology

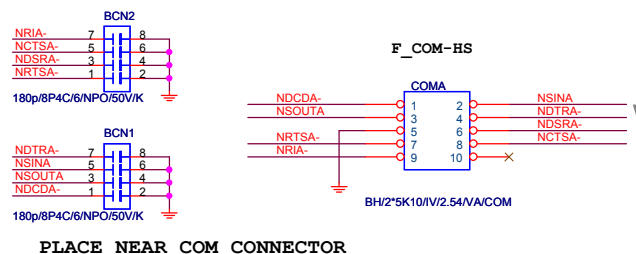
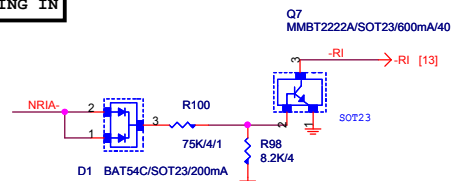
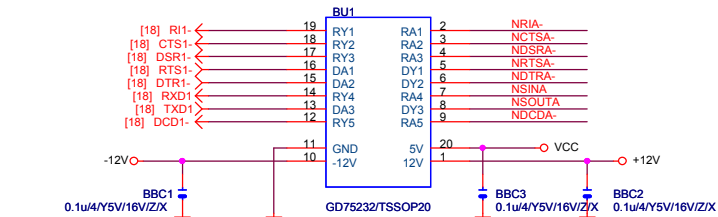
Title			
PCI EXPRESS X 4 PORT			
Size	Document Number	GA-H55M-UD2H	
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Date:	Thursday, November 05, 2009	Sheet	16 of 35

PCI1, 2 SLOT

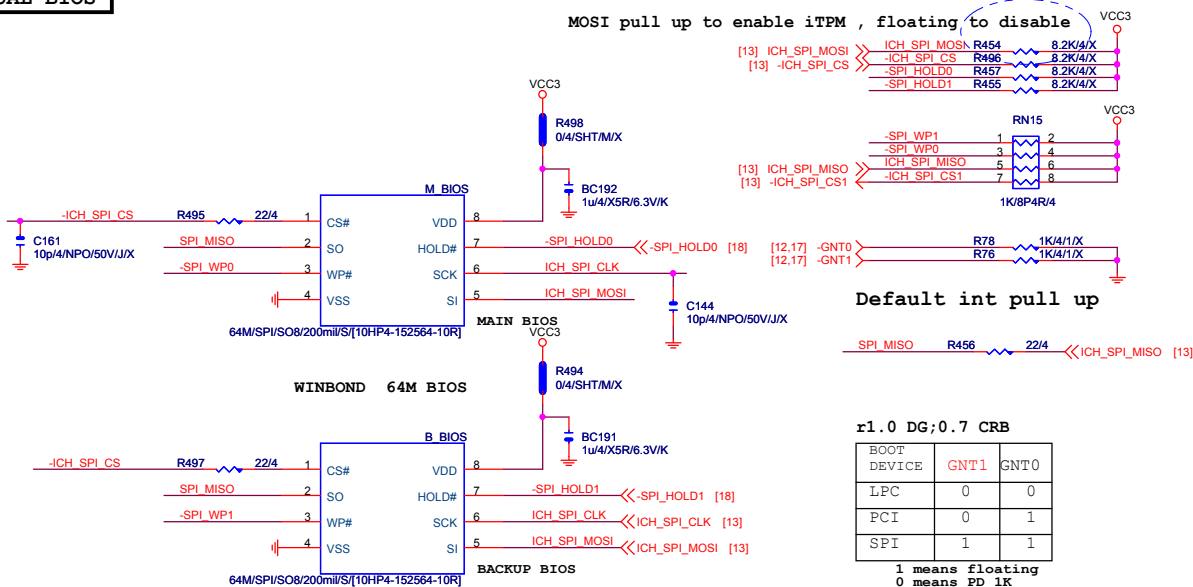


Gigabyte Technology			
Title			
PCI SLOT 1, 2			
Size			
Document Number			
GA-H55M-UD2H			
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1.01			
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RING IN



-PROHOT



Default int pull up

r1.0 DG;0.7 CRB

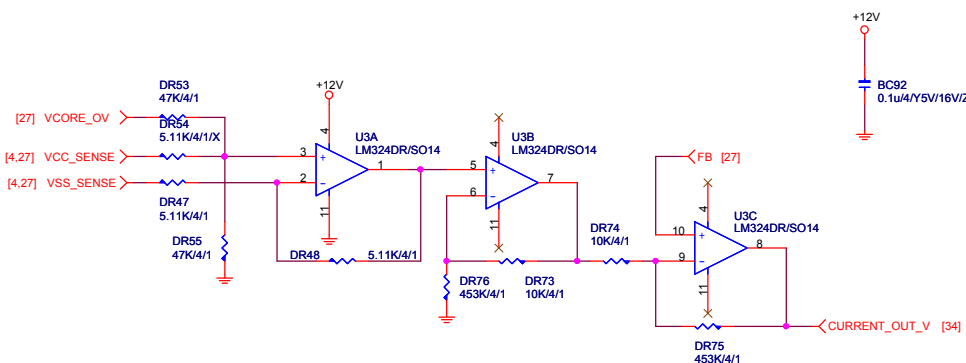
BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

1 means floating
0 means PD 1K

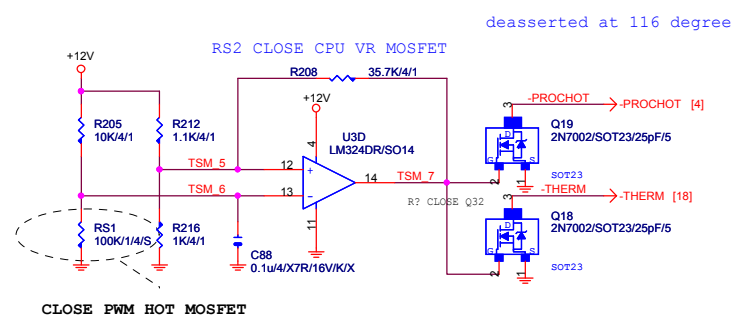
need to check which
is right

IC8SO-SOCKET

DYNAMIC CURRENT OC



-PROHOT



Gigabyte Technology

Title			
COM & PROHOT/Dynamic O.C.			
Size	Document Number		Rev
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20K/4/0.1% @ALC889A
20K/4/1% @ALC889A+/ALC888Vx

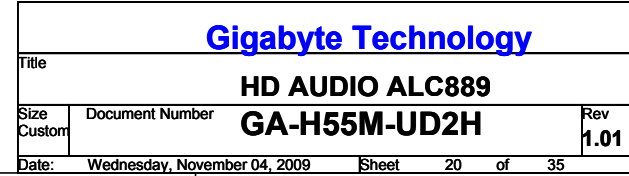
CR34 20K/4/1

CR65 10/4/X

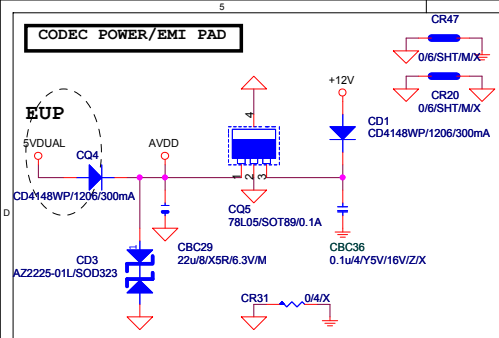
AVDD

21] CEN ←
21] LFE ←
21] S_SURR_L ←
21] S_SURR_R ←
21] SPDIF ←

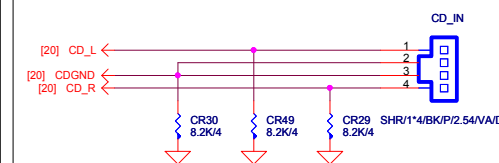
CBC31
470p/4/X7R/50V/K



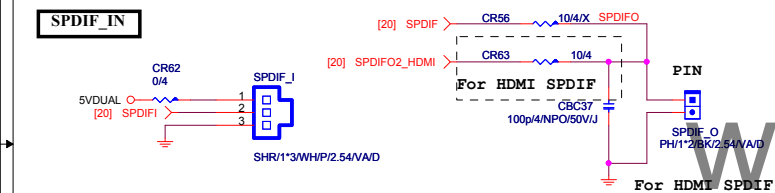
CODEC POWER/EMI PAD



CD IN

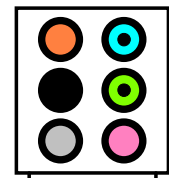


SPDIF IN

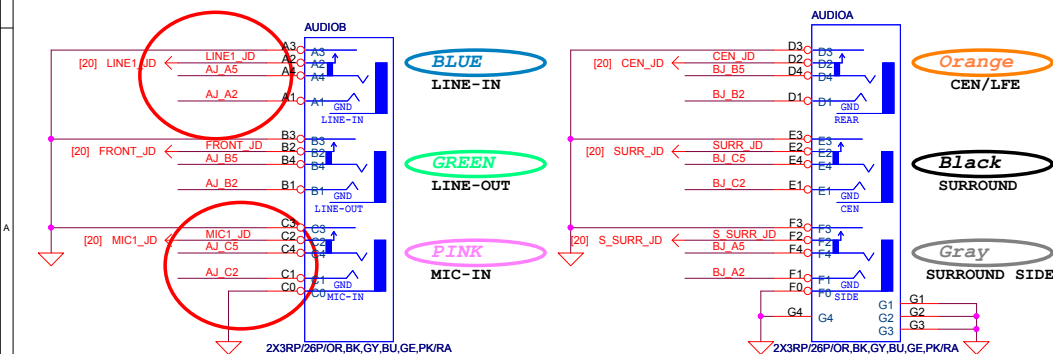


AZALIA JACK

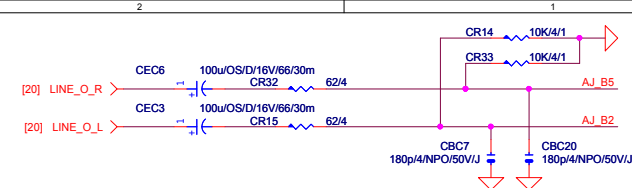
BTX AZALIA CONNECTOR



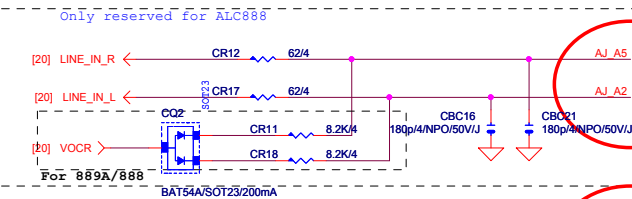
11NR6-403007-21R



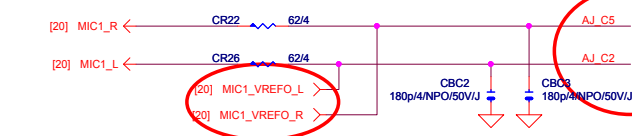
LINE-OUT



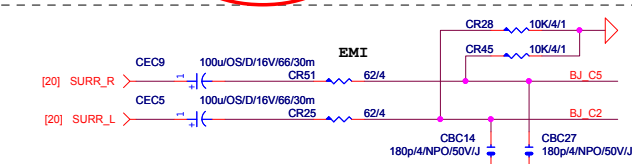
LINE-IN

Verify MIC function
in LINE-in

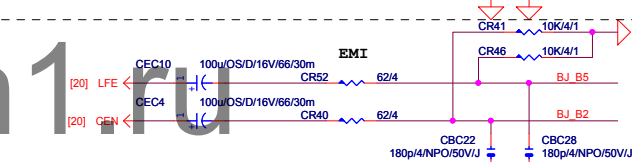
MIC-IN



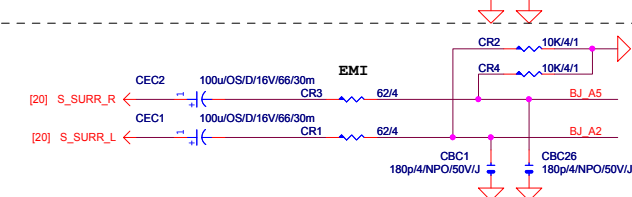
SURROUND



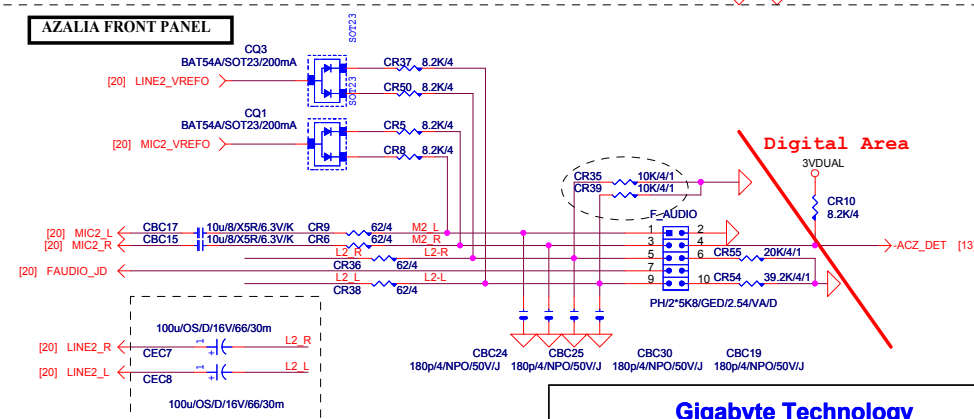
CEN/LFE



SURR BACK



AZALIA FRONT PANEL

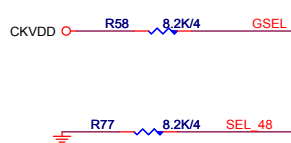
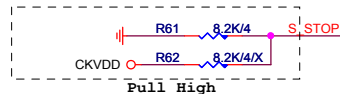
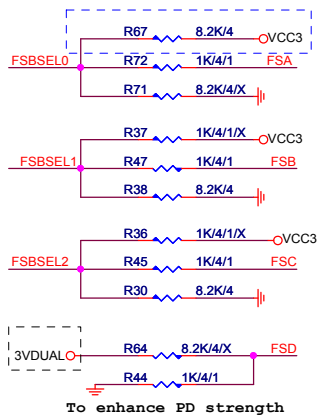
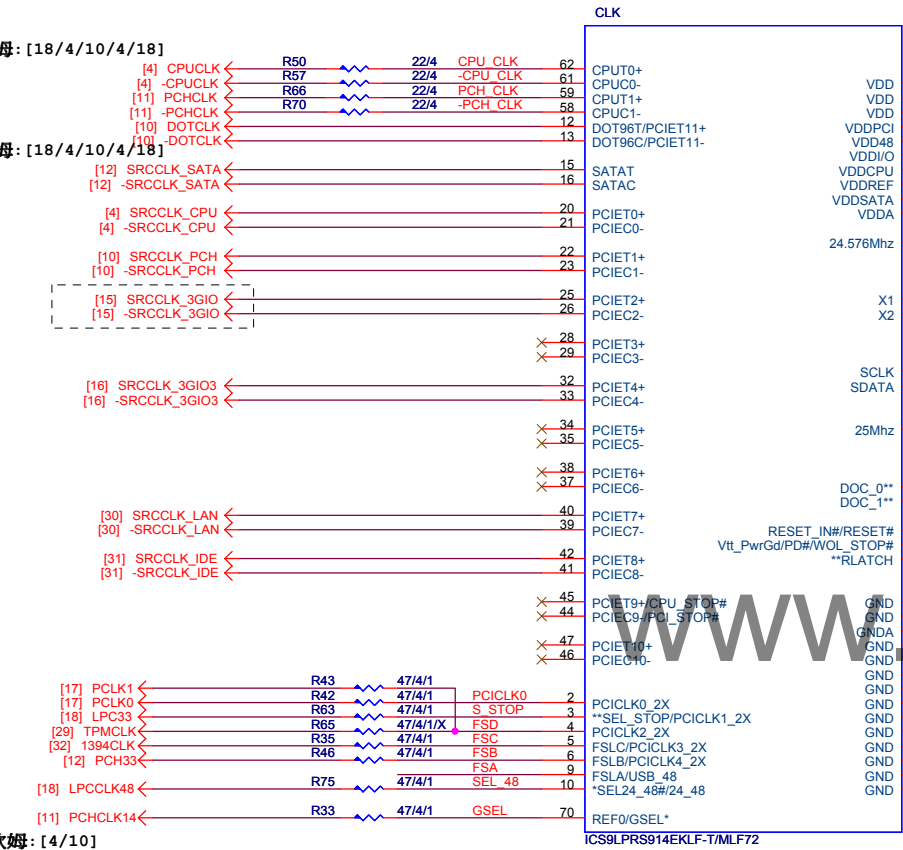


Gigabyte Technology		
AUDIO JACK		
GA-H55M-UD2H		
Rev	1.01	
Date:	Thursday, November 05, 2009	Sheet 21 of 35

50歐姆:[18/4/10/4/18]

50歐姆:[18/4/10/4/18]

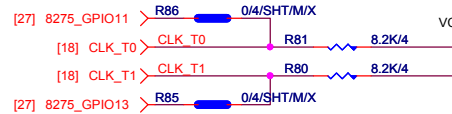
50歐姆:[4/10]



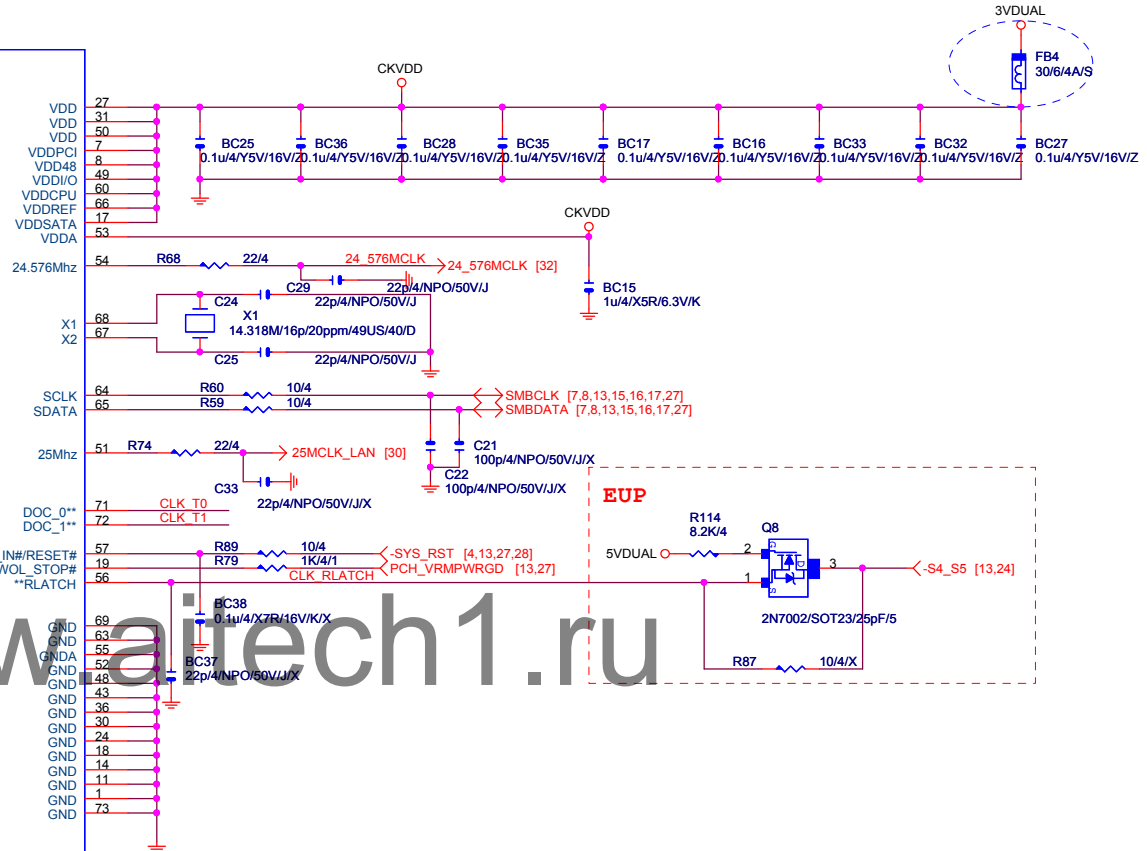
GSEL=1, 96Mhz from 12/13
GSEL=0, 100Mhz from 12/13

SEL_48=1, 24Mhz from pin10
SEL_48=0, 48Mhz from pin10

FSC	FSB	FSA	CPU
0	0	0	266MHz
0	0	1	133MHz
0	1	0	200MHz
0	1	1	166MHz
1	0	0	333MHz
1	1	0	400MHz

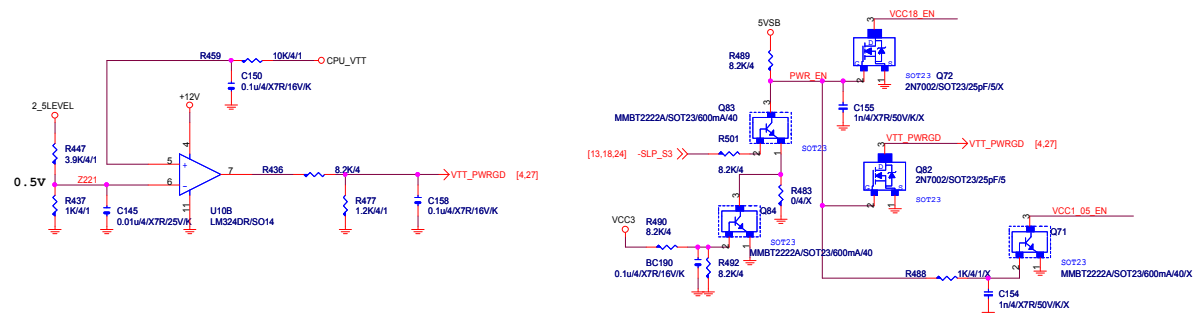
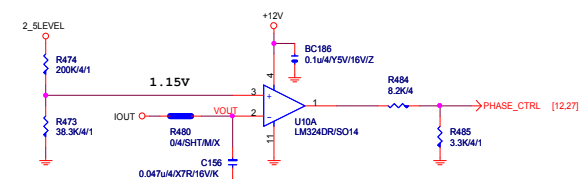
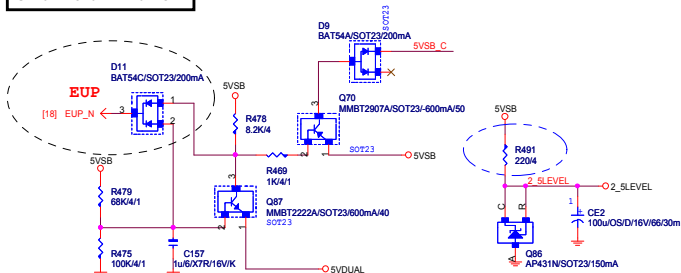
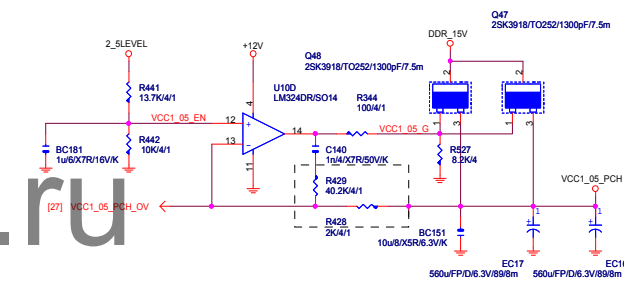
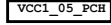
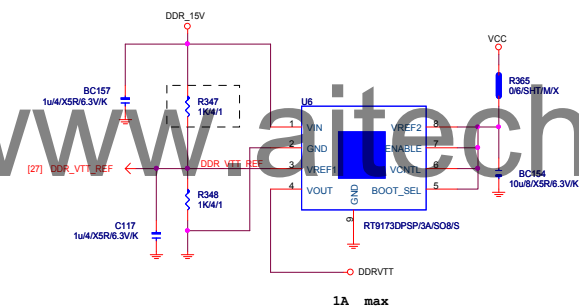
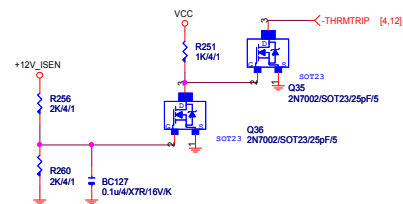
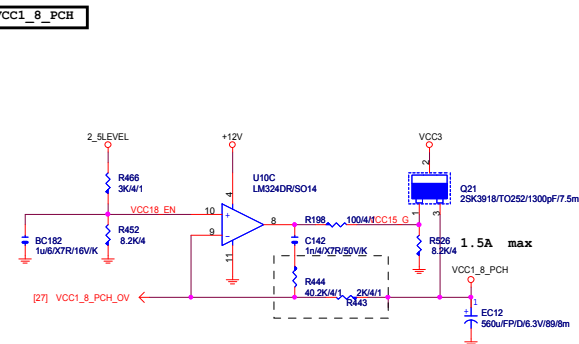
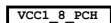
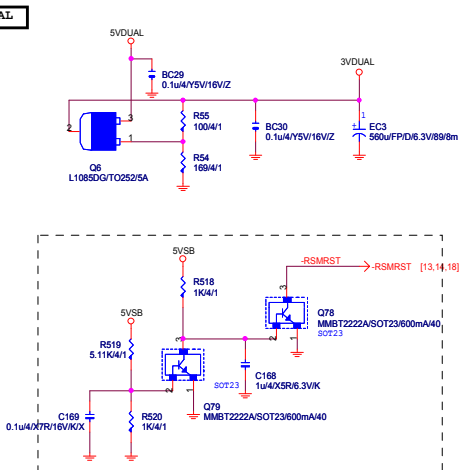
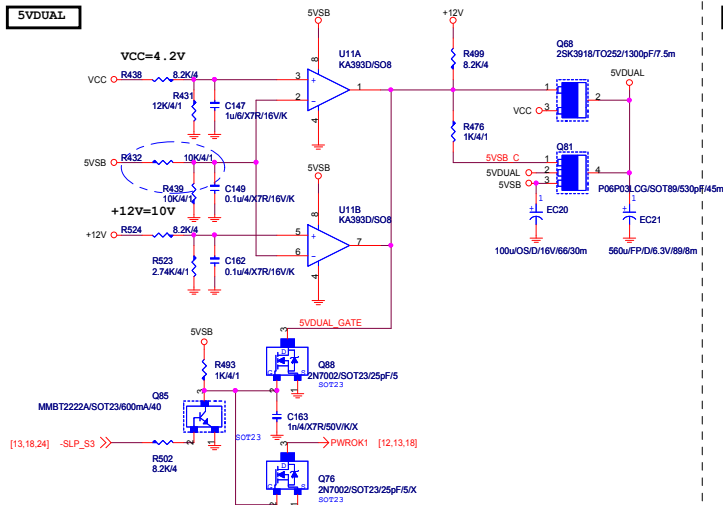


SEL_STOP: latched input to select pin functionality
1 = Selects pin 44/45 to be PCI_STOP#/CPU_STOP#
0 = Selects pin 44/45 to be PCIE outputs;
3.3V PCICLK output

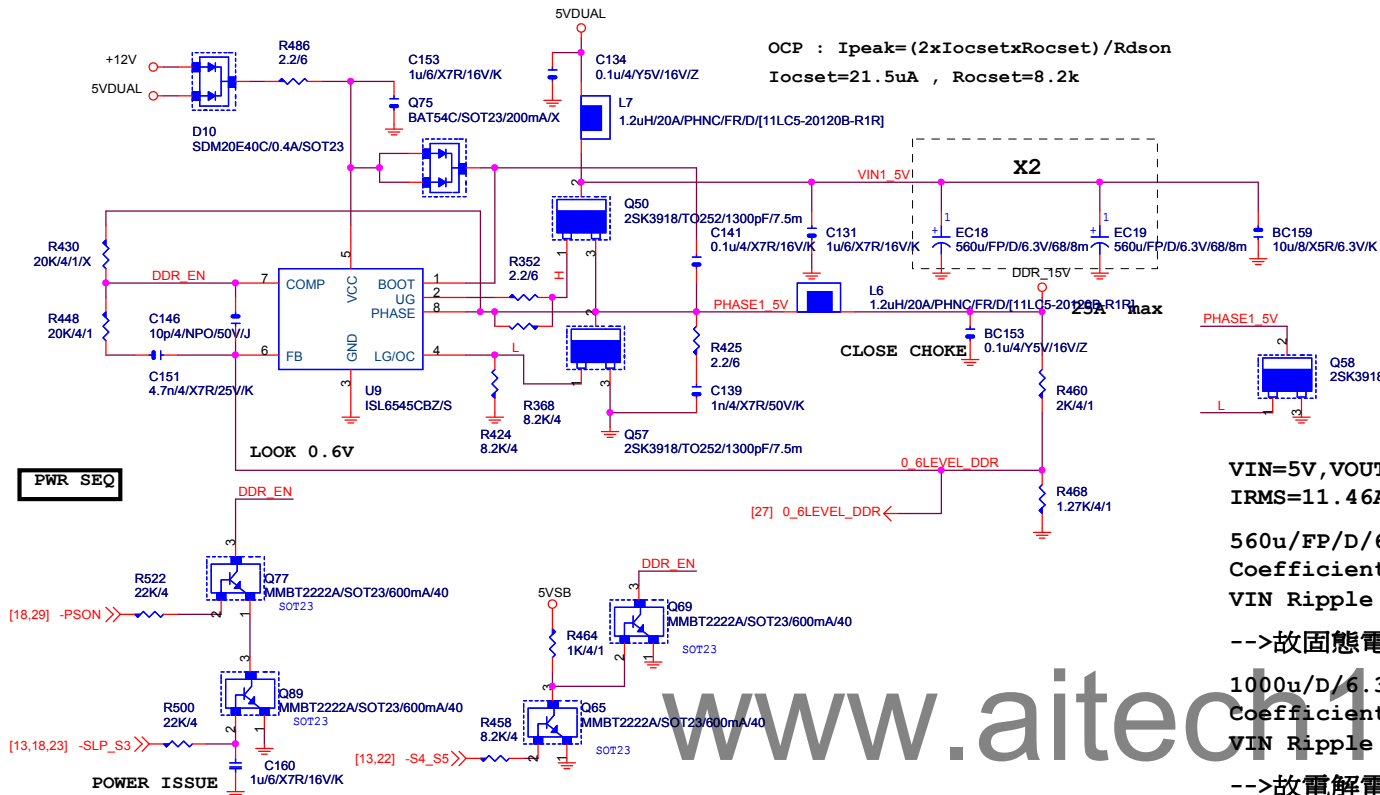


Gigabyte Technology

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CK505 CLK GEN			
GA-H55M-UD2H			
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DDR1_5V



$$OCP : I_{peak} = (2 \times I_{ocset} \times R_{ocset}) / R_{dson}$$

$$I_{ocset} = 21.5\mu A, R_{ocset} = 8.2k$$

VIN=5V, VOUT=1.5V, IOUT=25A, PHASE=1
IRMS=11.46A

560u/FP/D/6.3V/68/8m RIPPLE CURRENT=5.6A
Coefficient=1.7(85°C), 1(105°C)
VIN Ripple current=5.6X1.7=9.52A(85°C)

-->故固態電容須 $2 \times 9.52 = 19.04 > 11.46A$

1000u/D/6.3V/8C/30m RIPPLE CURRENT=1.14A
Coefficient=1.7(85°C), 1(105°C)
VIN Ripple current=1.14X1.7=1.938A(85°C)

-->故電解電容須 $6 \times 1.938 = 11.628 > 11.46A$

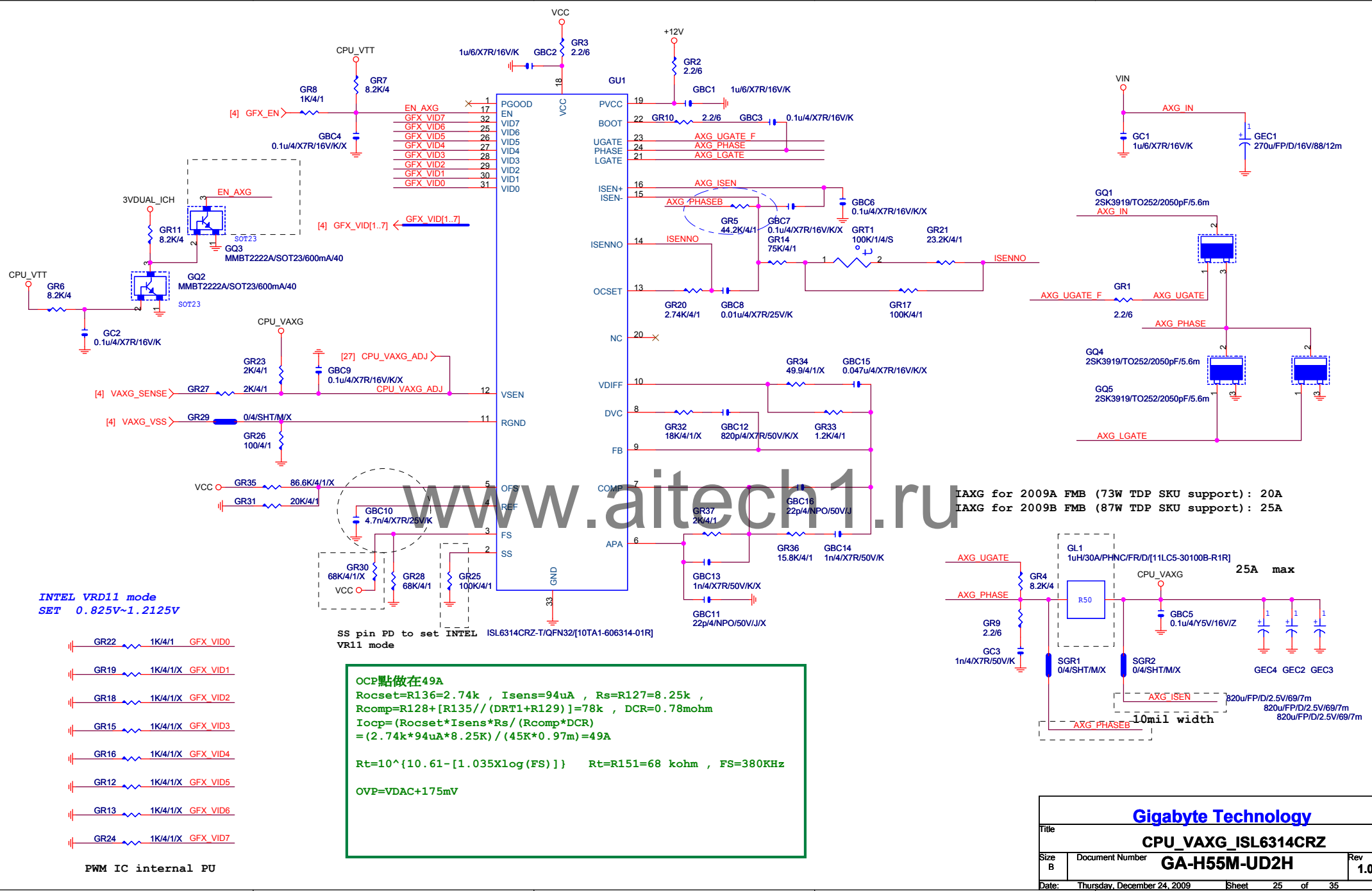
VIN=3V, VOUT=1.05V, IOUT=7.5A, PHASE=1
IRMS=3.5A

-->故固態電容須 $1 \times 9.52 = 9.52 > 3.5A$

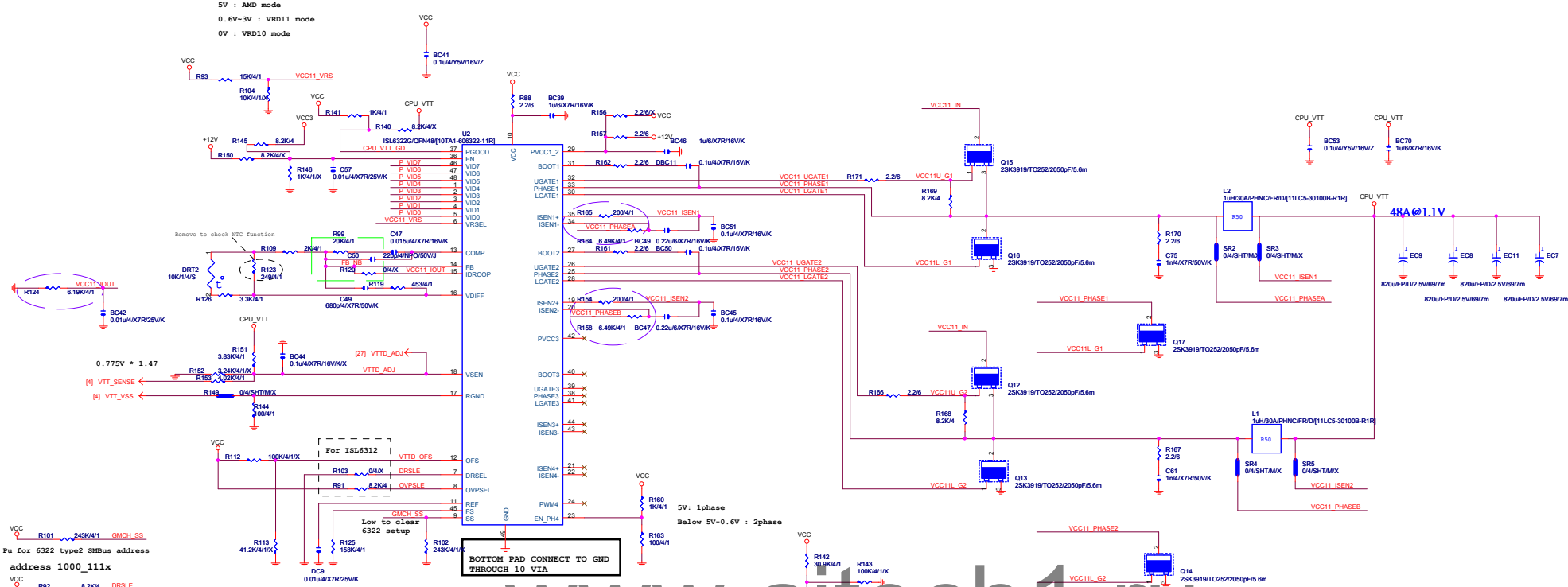
-->故電解電容須 $2 \times 1.938 = 3.876 > 3.5A$

Gigabyte Technology

Title			DDR_15V
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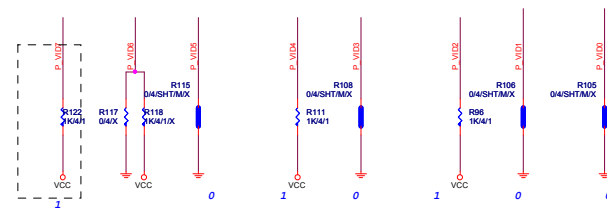
5V : AMD mode
0.6V~3V : VRD11 mode
0V : VRD10 mode



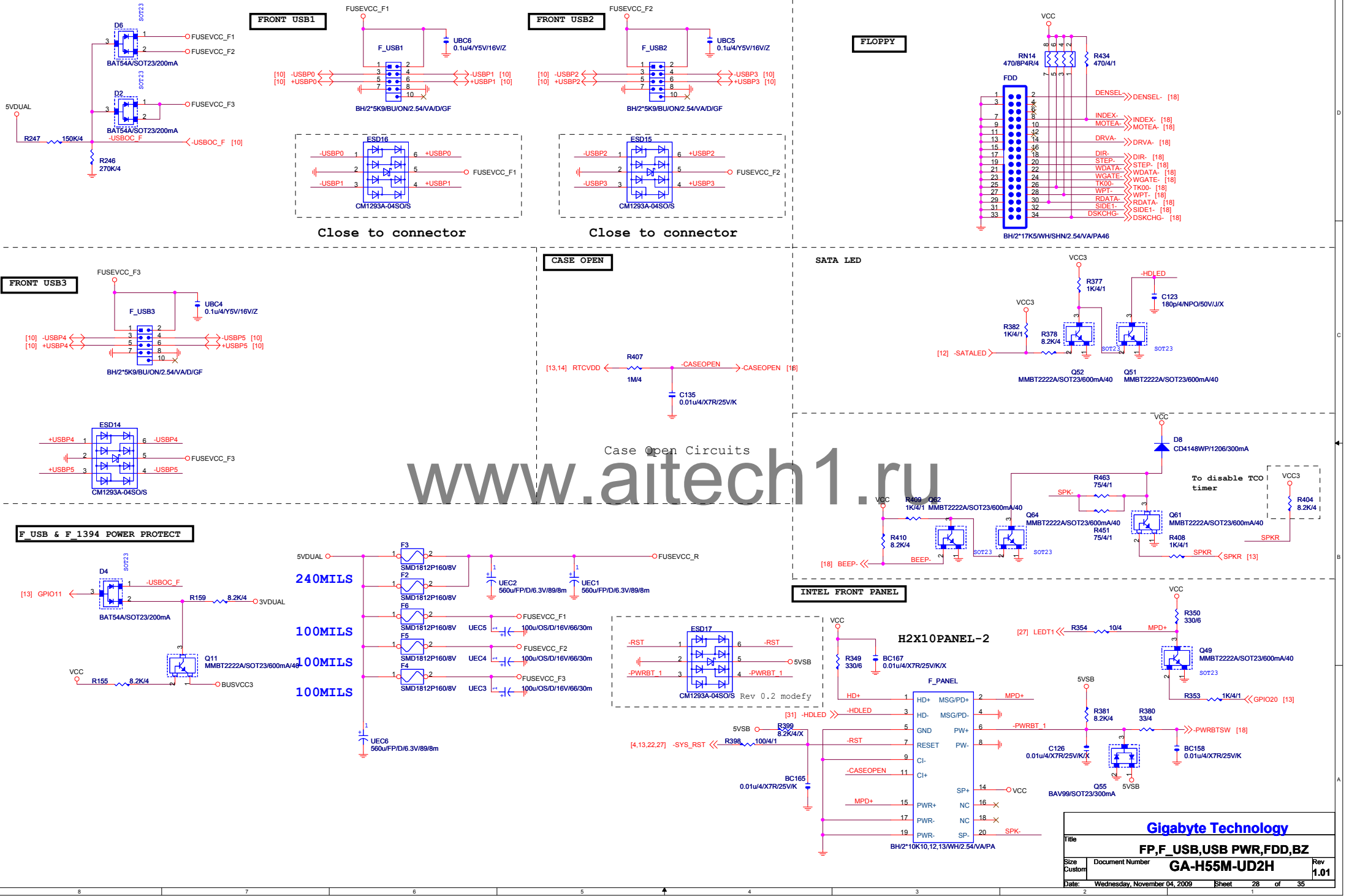
OCF點做在146A
Isensx R270阻值設在590ohm
 $I_{ocp} = (I_{sensx} R_{isensxPhase}) / DCR$
 $= [(120uA \times 590X2) / 0.97] = 146A$
 $L / DCR = R + C$
 $L = 1uH$ $DCR = 0.97m\Omega$ $1uH / 0.97m\Omega = 4.7k\Omega$ $0.22uF$
 R_{isensx} R260 阻值=4.7k ohm, C_{isensx} BC75=0.22uF
 $R_t = 10^4 [10.61 - [1.035X \log(FS)]]$ $R_t = R301 = 158k\Omega$, $FS = 170KHz$
 $OVP = V_{DAC} + 225mV$

1.05V / 1.1V select by CPU

Bit 7 Pull High for AMD 6bit mode
Recover Bit6 when use AMD mode
AMD 6bit mode
SET 1.05V
[1x010100]

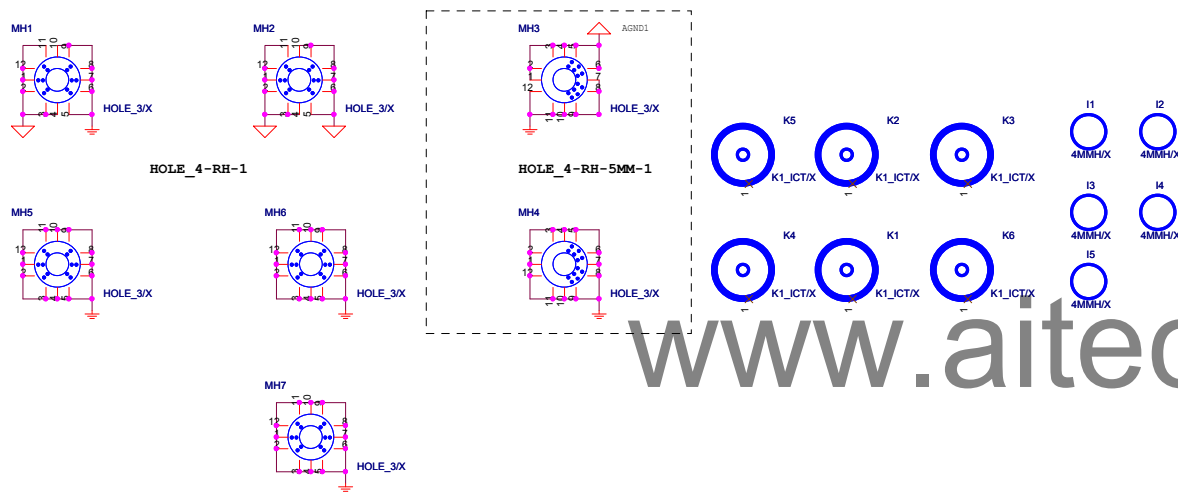
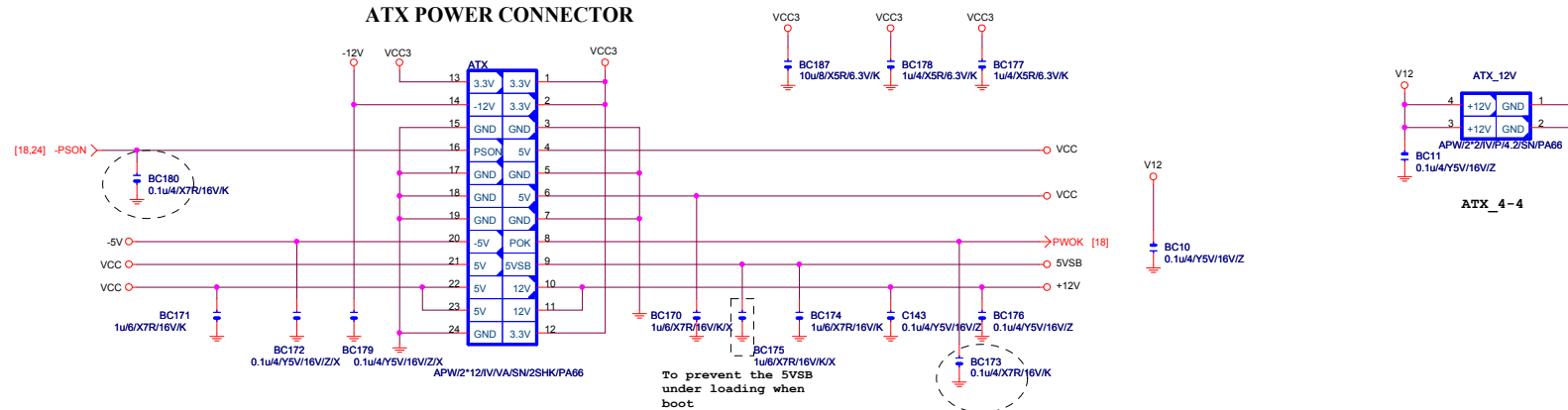


VIN=5V, VOUT=1.1V, IOUT=48A, PHASE=2
IRMS=11.91A
560uF/FP/D/6.3V/68/8m RIPLE CURRENT=5.6A
Coefficient=1.7(85°C), 1(105°C)
VIN Ripple current=5.6X1.7=9.52A(85°C)
-->故固態電容須2X9.52=19.04>11.91A
1000uF/D/6.3V/8C/30m RIPLE CURRENT=1.14A
Coefficient=1.7(85°C), 1(105°C)
VIN Ripple current=1.14X1.7=1.938A(85°C)
-->故電解電容須7X1.938=13.566>11.91A

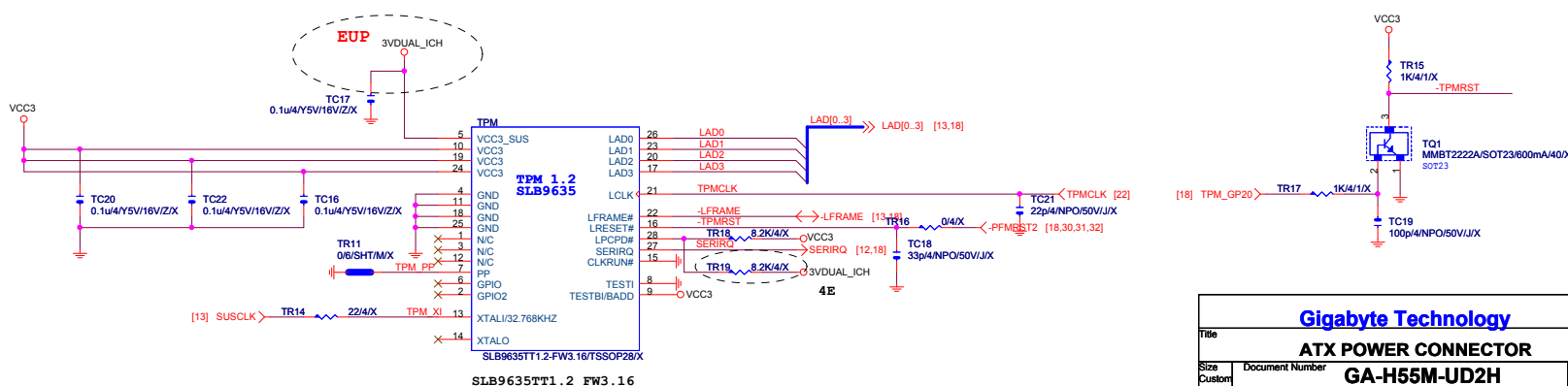


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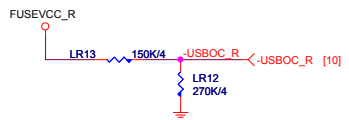
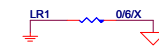
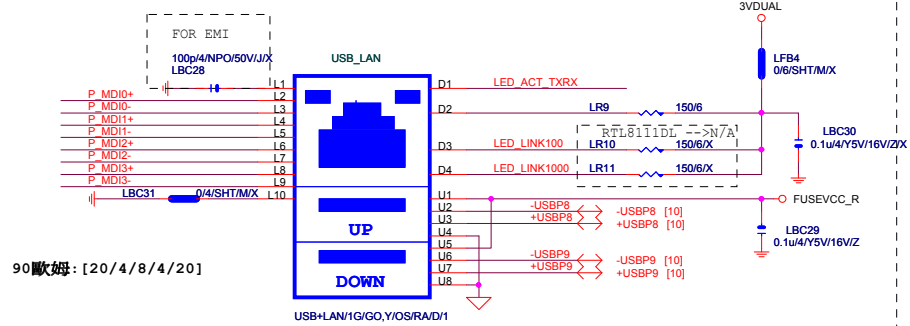
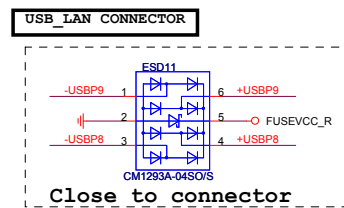
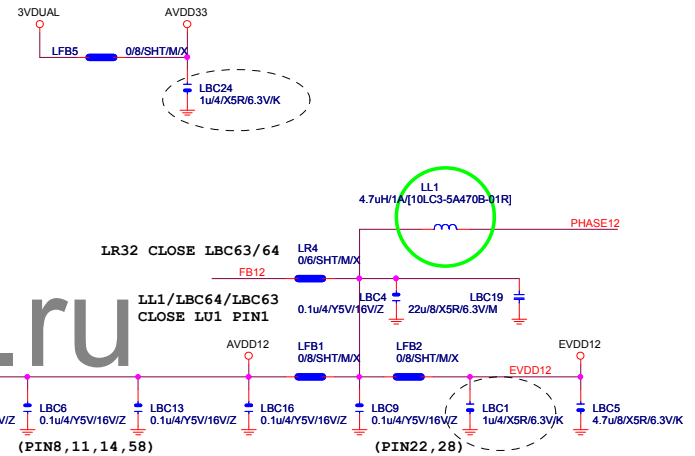
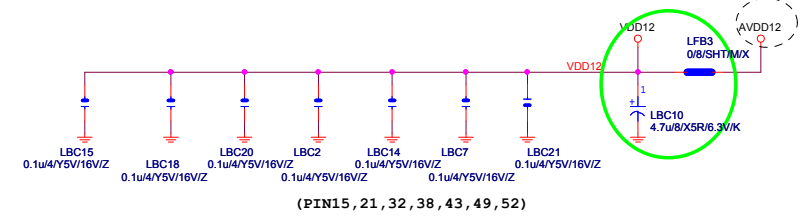
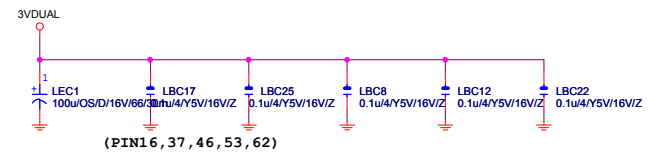
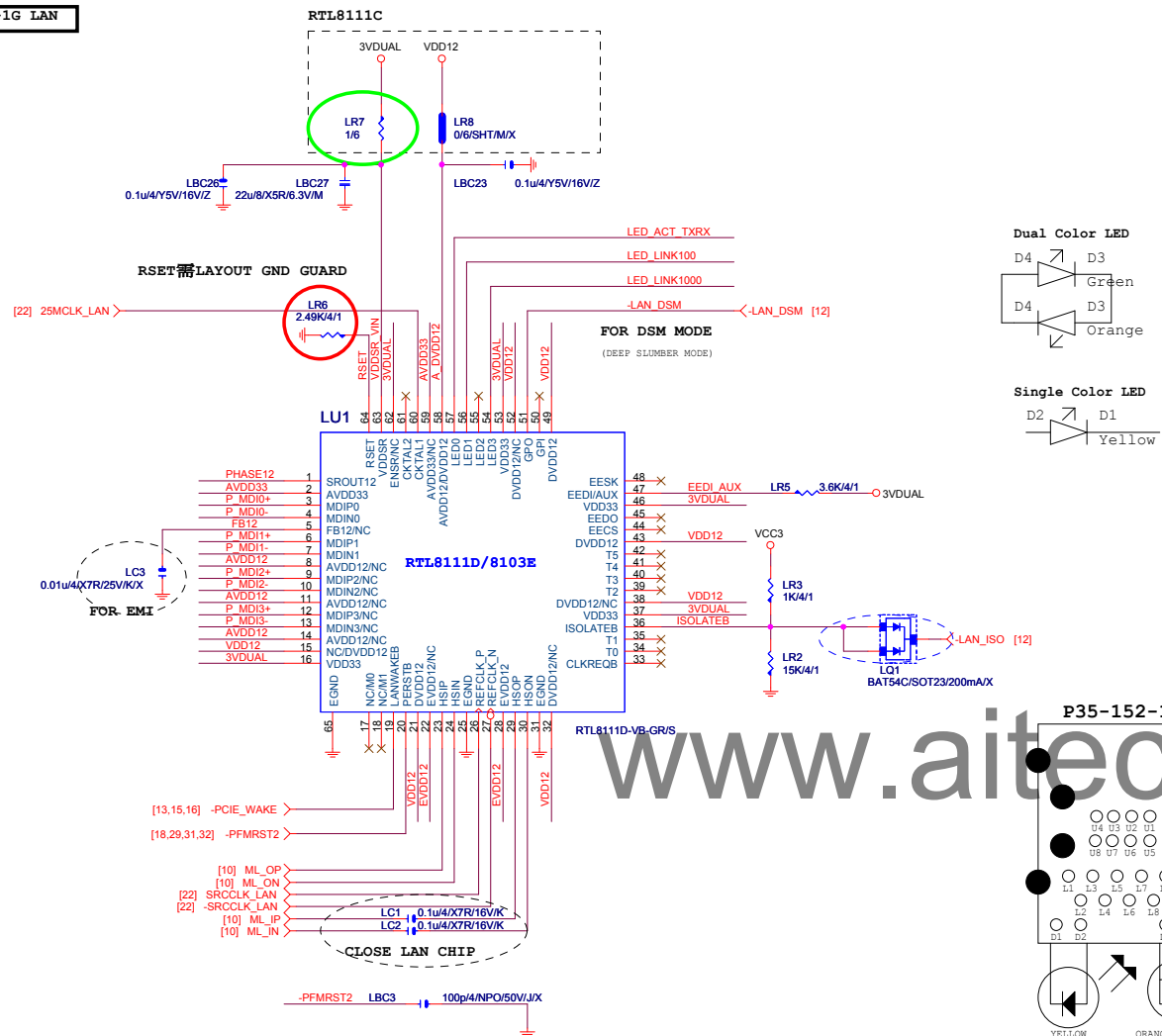
ATX POWER CONNECTOR



TPM

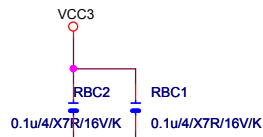
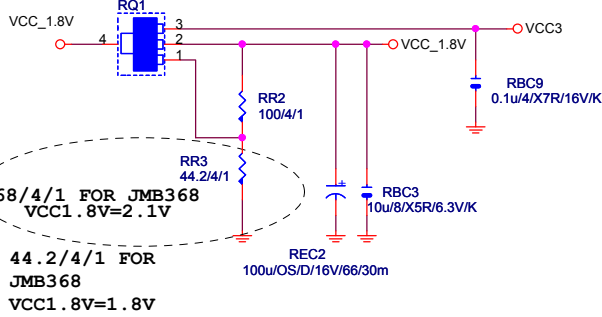


PCIE-1G LAN

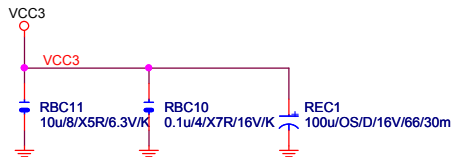


3.3V to 1.8V Voltage Regulator

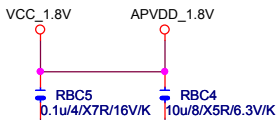
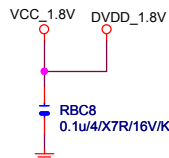
L1117LGN/SOT223/1A



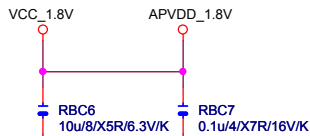
close to IC



Close to pin22 and pin39



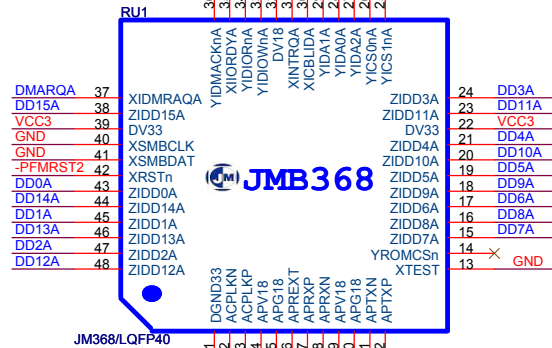
CLOSE TO pin22



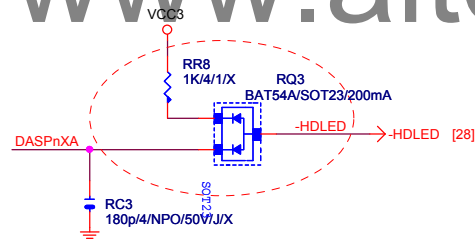
close to pin17

[18,29,30,32] -PFMRST2

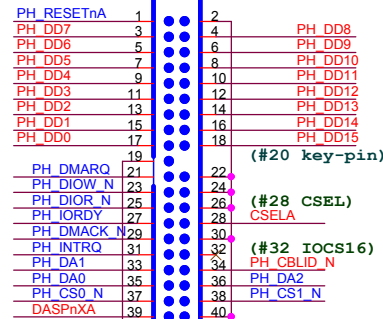
RC4
100p/4/NPO/50V/J/X



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IDE Connector



BH/2*20K20/WH/SHN/2.54/VA/PA66

PH DD7 DD7A
PH DD8 DD8A
PH DD6 DD6A
PH DD9 DD9A

PH DD5 DD5A
PH DD4 DD4A
PH DD10 DD10A
PH DD11 DD11A

PH DD3 DD3A
PH DD12 DD12A
PH DD2 DD2A
PH DD13 DD13A

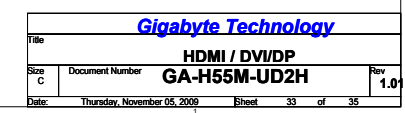
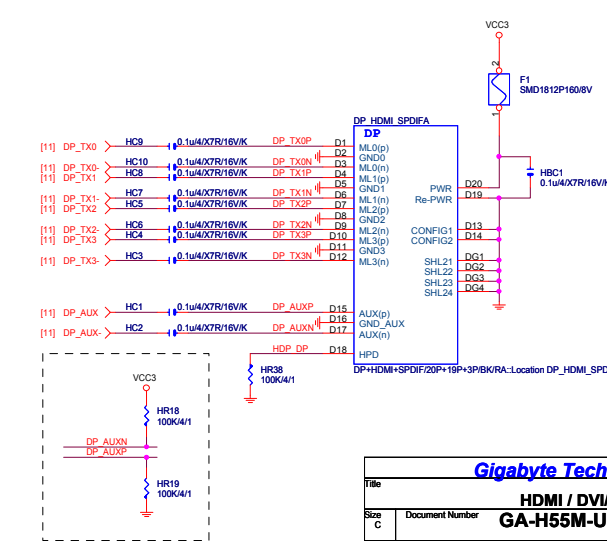
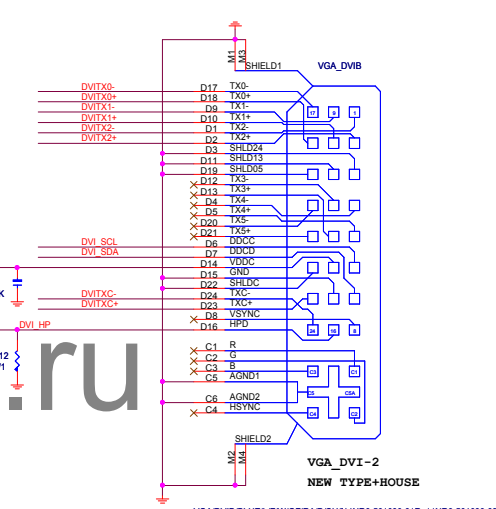
PH DD1 DD1A
PH DD0 DD0A
PH DD14 DD14A
PH DD15 DD15A

PH DIOW_N DIOWnA
PH DIOR_N DIORnA
PH DMACK_N DMACKnA
PH DA1 DA1A
PH DA0 DA0A
PH CS0_N CS0nA
PH DA2 DA2A
PH CS1_N CS1nA

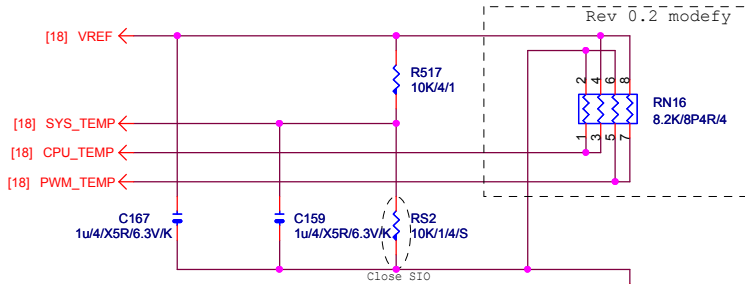
PH IORDY IORDYA
PH DMARQ DMARQA
PH INTRQ INTRQA
PH CBLID_N PDIAGnA

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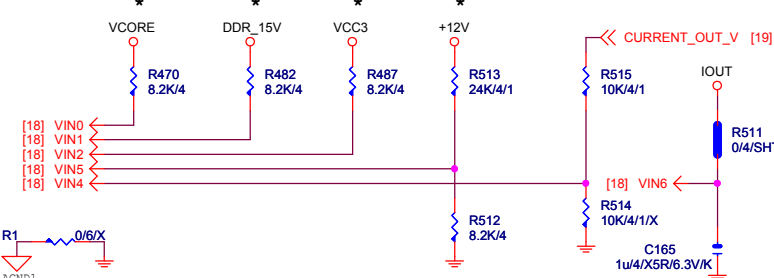
Title			JMR368
Size	Document Number	GA-H55M-UD2H	
Custom			1.01
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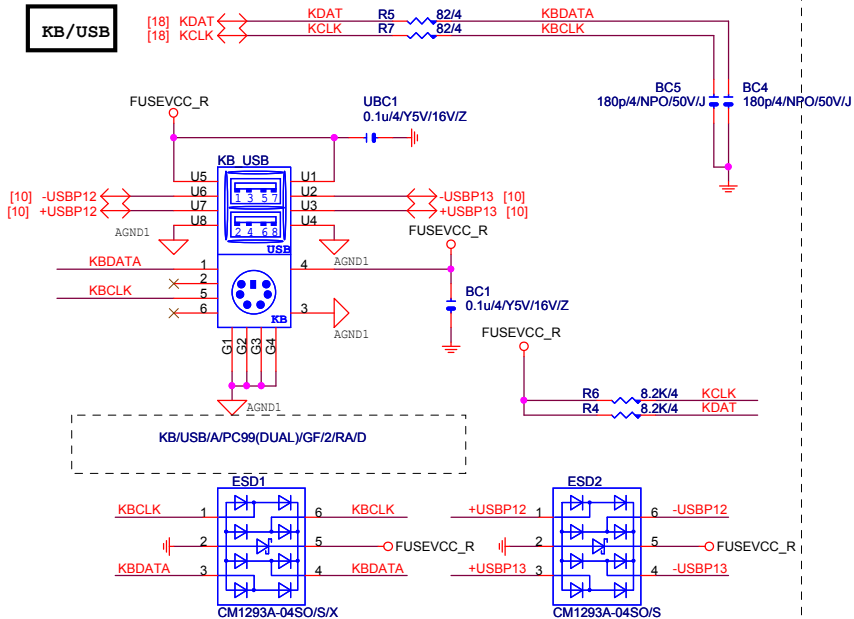
TEMP H/W MONITOR



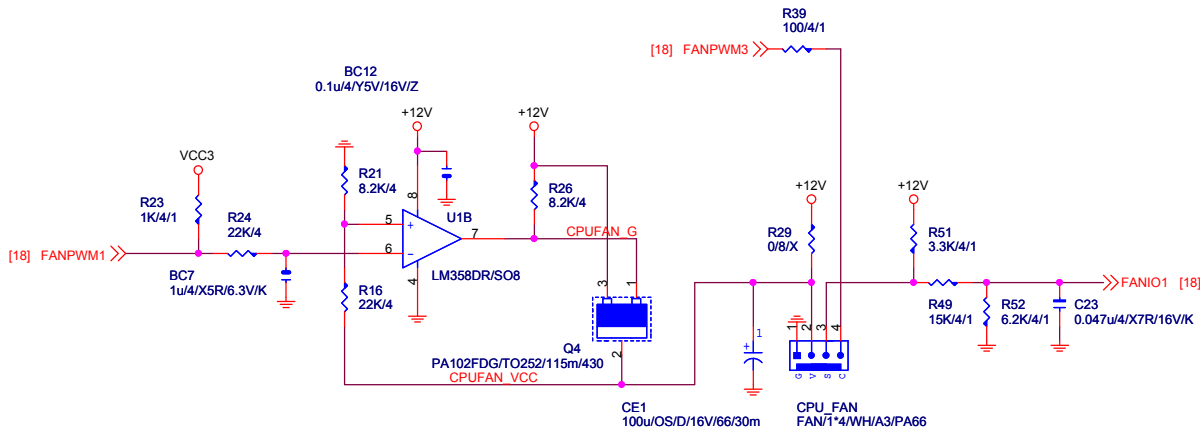
VOLTAGE-- H/W MONITOR



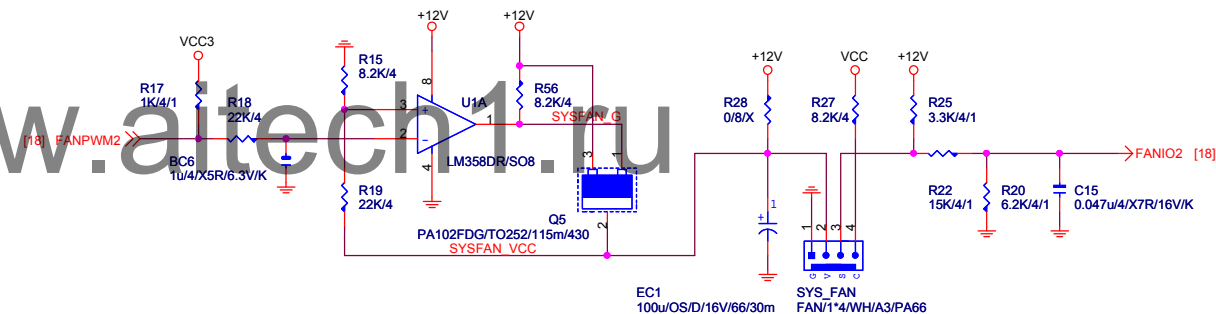
KB/USB



CPU SMART FAN



SYS SMART FAN Linear SYS_FAN



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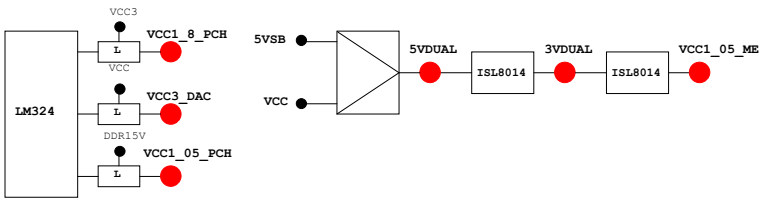
Title			HWM,KB/MS, FAN CTRL
Size	Document Number	GA-H55M-UD2H	
Custom		Rev 1.01	
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PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI	-PECI_REQ	N/A
GP1/TACH1	MAIN		GPI	ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI	ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO	GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE	OC5#	N/A
GP10/OC6#	STBY		NATIVE	OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	-SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI	GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	OC7#	N/A
GP15	STBY	L	GPO	GPIO15	N/A
GP16	MAIN		GPI	-SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE	MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI	-LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE	LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI	VCC18_PCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN		NATIVE	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO	TLS	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE	-CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE	-AC2_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI	N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO	MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO	LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI	-LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI	N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI	VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	-LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE	OC1#	N/A
GP41	STBY		NATIVE	OC2#	N/A
GP42	STBY		NATIVE	OC3#	N/A
GP43	STBY		NATIVE	OC4#	N/A
GP44	STBY	L	NATIVE	N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	-LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE	PSI_LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN	EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN	VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE	1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

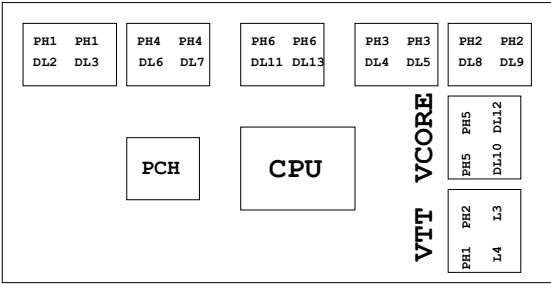
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SEN	LOW_PWR_1	
VIDO5/GP27/SEN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSB5W#/GP40	CSI_F0	BSEL166_1
SUSCH#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMB_C_R	SEC_PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMB_C_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VIDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下:



BIOS超電壓對應表:

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號:

8IBP:
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組) 包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH